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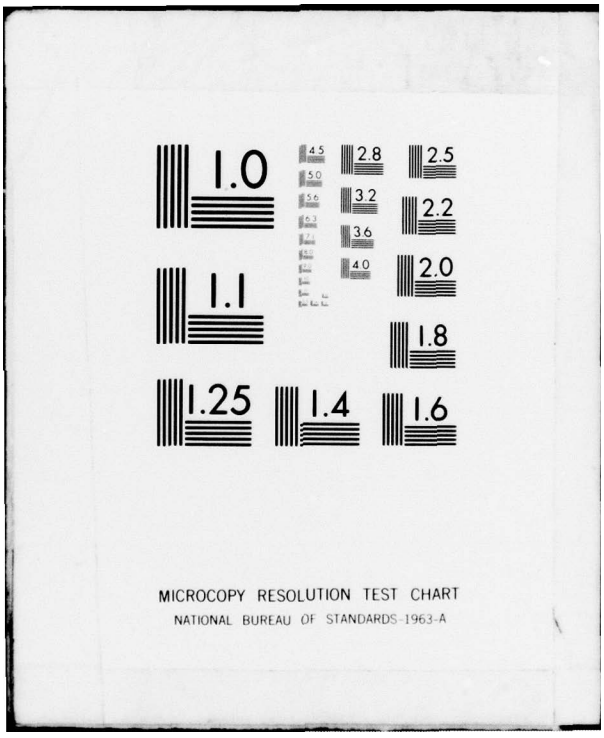
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Interim Report
June 1979

ANALOG BINARY PROGRAMMABLE TRANSVERSAL FILTER

RCA

D. A. Gandolfo
J. R. Tower

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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Correlators
Signal Processing

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this program is to develop a programmable CCD (Charge-Coupled Device) circuit capable of correlating a variety of binary-coded waveforms. This analog-binary correlator will store a binary waveform as a reference, and will then compare newly arriving signals to the reference waveform. In general, the signal will be a binary code that has been corrupted in the transmission channel so that upon arrival at the receiver, it really has an analog character (i.e., the amplitude varies continuously). Analog-binary correlation techniques have an important advantage over

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purely digital approaches. If the analog signal is directly compared to the reference, only a single correlation channel is required, whereas a digital correlator requires a separate channel for each bit of resolution in the analog-to-digital converter. Thus, a reduction in parts count, with attendant improvements in size, cost and reliability, is realized with the CCD correlator.

The correlator is an important device because correlation of binary waveforms is a function widely used in spread spectrum systems, which offer important advantages for military communications and radar applications. Spread spectrum advantages include jam resistance, reduced detectability and improved signal-to-noise ratio for given transmitter power. Thus, the device whose design is described here should be broadly useful in military systems.

Specified and expected performance of the analog-binary programmable transversal filter device are summarized below:

Performance Parameter	Contract Requirement	RCA Design Goal
Number of Points Correlated	512	512, 256, 128, 64
CCD Clock Rate	8 MHz	10 MHz
Reference Code Load Rate (Program Register)	0.5 MHz	5 MHz
Dynamic Range (Single Tap)	35 dB	45 dB
Signal-to-Noise Ratio (Single Tap)	50 dB	66 dB
Charge Transfer Inefficiency ($n\epsilon$)	0.2	0.1

A further objective of the program is to simplify the interface between the CCD correlator and the surrounding system by including many support circuits on the CCD chip. Support circuits include clock drivers, reference code load logic and TTL-MOS level translators.

This report includes a general description of the analog-binary programmable transversal filter device, designated TC1235 (Section 2) and a detailed discussion of the design of all the circuits on the chip (Section 3). Section 2 includes: a brief description of earlier devices, the manner in which the CCD correlator operates, correlator interfaces with off-chip circuits, and timing information. Section 3 includes: a description of the buried channel CCD/NMOS process with self-aligned diffusions, and detailed circuit designs. Particular attention is given to major features which were not included in earlier correlator designs. These are the tap structure, uniphase clocking, and a corner-turning circuit. The tap structure is believed to be highly significant in that it eliminates the code-dependent bias problem. In earlier correlator designs, the correlation signal is superimposed on a bias current which is independent of the signal, and which depends on the number of ones and zeroes in the code. As a result, the bias signal changes when the code is changed. This problem surfaced early in the design study phase of the program, and considerable subsequent effort was expended working out a design that was first proposed by the MIT Lincoln Laboratory. With this tap circuit, the new correlator will not be limited to balanced codes; i.e., codes containing equal numbers of ones and zeroes.

PREFACE

The work discussed in this document was performed under Air Force Contract F19628-77-C-0263, "Analog-Binary Programmable Transversal Filter". This is an Interim Report (CDRL Sequence Number 102, Line Item 0002) covering the period from 9/30/77 through 8/31/78. RCA Government Systems Division, Advanced Technology Laboratories in Camden, NJ, is the organization responsible for the work. Dr. D. A. Gandolfo was the principal investigator. The work was monitored by Dr. F. D. Shepherd and Dr. L. H. Skolnik, Electronic Systems Division, Deputy for Electronics Technology, Hanscom AFB, MA.

The report was prepared by D. A. Gandolfo and J. R. Tower. The following RCA personnel contributed to the work discussed: J. R. Tower, J. I. Pridgen, D. A. Gandolfo (Advanced Technology Laboratories); R. Angle, D. Sauer, F. Shallcross (RCA Laboratories, Princeton). A valuable contribution (a new tap structure design) was made by S. C. Munroe of the MIT Lincoln Laboratory.

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (cont'd.)

TABLES

Section 1.0

INTRODUCTION and SUMMARY

The objective of this program is to develop a programmable CCD (Charge-Coupled Device) circuit capable of correlating a variety of binary-coded waveforms. This analog-binary correlator will store a binary waveform as a reference, and will then compare newly arriving signals to the reference waveform. In general, the signal will be a binary code that has been corrupted in the transmission channel so that upon arrival at the receiver, it really has an analog character (i.e., the amplitude varies continuously). Analog-binary correlation techniques have an important advantage over purely digital approaches. If the analog signal is directly compared to the reference, only a single correlation channel is required, whereas a digital correlator requires a separate channel for each bit of resolution in the analog-to-digital converter. Thus, a reduction in parts count, with attendant improvements in size, cost and reliability, is realized with the CCD correlator.

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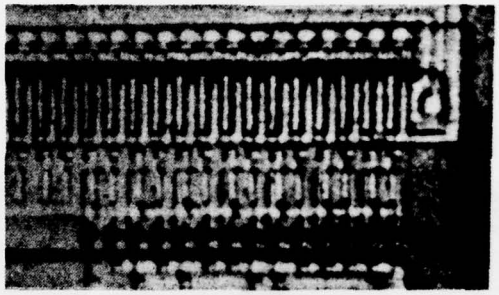
The period covered by this report concluded with the completion of the correlator design. Circuit design, simulation, layout and digitizing were finished, and a computer tape was produced which contains the circuit designer's inputs to the photomask fabrication process. The next report on this program will discuss photomask fabrication, wafer processing, and device test and evaluation.

Section 2.0

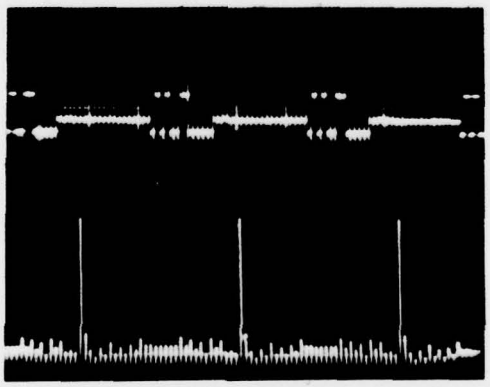
GENERAL DESCRIPTION of ANALOG-BINARY CORRELATOR

2.1 CCD CORRELATOR EVOLUTION

The analog-binary correlator (TC1235), designed under this contract, was preceded by several generations of CCD correlators at RCA. The earlier devices were: (1) TC1102 — a 13-bit, Barker-coded device with fixed (hard-wired) taps, demonstrating the utility of floating-gate taps; (2) TC1180 — the first programmable CCD correlator[1, 2], a 64-bit device with programmable floating-gate taps; (3) TC1221 — a 128-stage device with selectable code lengths (16, 32, 64, 128 bits) and on-chip clock drivers, as well as programmable taps. Each succeeding device exhibited important growth in capability over its predecessors. The TC1235 correlator, with greater length, more on-chip support circuits and improved tapping and clocking schemes, continues this growth. The salient features of the TC1102, 1180 and 1221 correlators are illustrated in Figs. 2-1. -2 and -3.

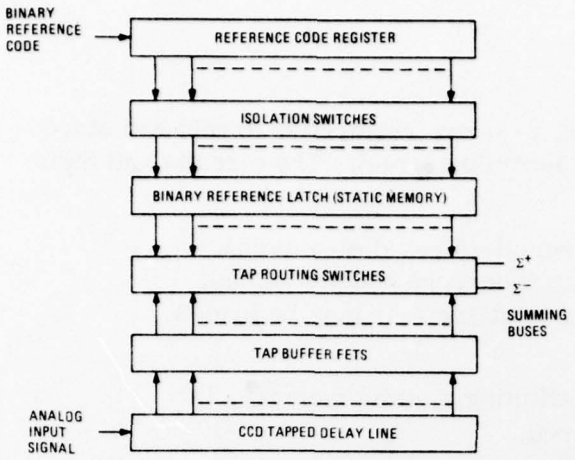


a. Photomicrograph. This CCD tapped delay line employs floating-gate taps. The taps are hard-wired to summing buses, and the device is not programmable.

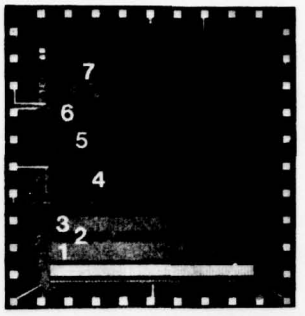


b. Performance. Correlation (lower trace) observed with 13-bit Barker-code input (upper trace). Correlation is close to theoretical, with near unity-level sidelobes and a 13:1 peak-to-sidelobe ratio.

Fig. 2-1. Characteristics and performance of TC1102 Barker-coded correlator with fixed taps.

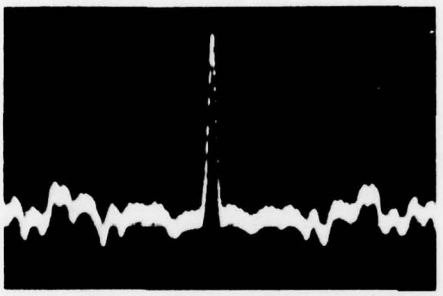


a. Device Architecture. These are the basic correlation circuits; i.e., the elements required for loading and storing a reference code and comparing it to a received signal.



1. CCD tapped delay line
2. Tap buffer FETs
3. Tap switches
4. Static memory
5. Isolation switches
6. Buffer amplifiers
7. Reference code input register

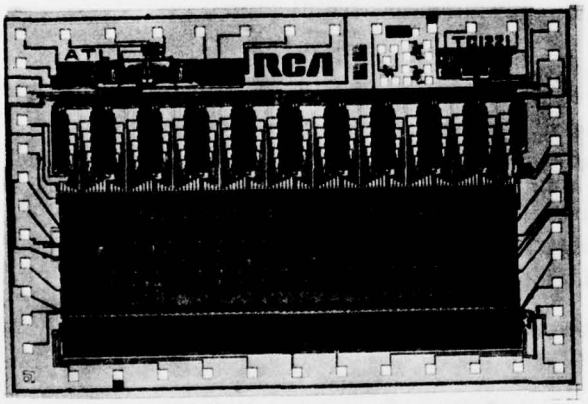
b. Photomicrograph. The CCD is a two-phase, shallow buried-channel device with Al and poly-Si gates. NMOS technology is used for the other circuits. The program register operates at 5 MHz and the CCD TDL (tapped delay line) operates at up to 20 MHz.



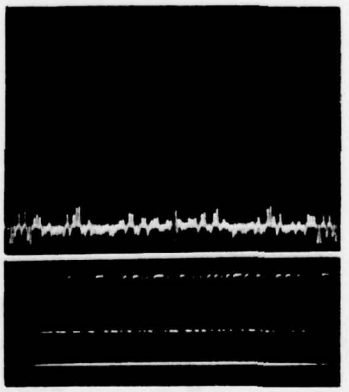
- 7:1 PEAK-TO-SIDELOBE RATIO (THEORETICAL = 7.1:1)
- TAP UNIFORMITY: 2% RMS
- TAP LINEARITY: 2ND & 3RD HARMONICS 45 dB BELOW FUNDAMENTAL WITH INPUT SIGNAL 60% OF FULL WELL (PEAK-TO-PEAK)
- CCD OPERATION TO 20 MHz WITH LOW TRANSFER LOSS ($\epsilon < 10^{-4}$ AT 10 MHz)
- PROGRAM REGISTER OPERATION TO 5 MHz (15 μSEC REQUIRED FOR CODE CHANGE)

c. Performance. Correlation of a 64-bit bi-phase code at 10 Mb/s data rate.

Fig. 2-2. Characteristics and performance of TC1180 programmable analog-binary correlator.



a. *Photomicrograph.* The TC1221, a 128 stage correlator. The basic correlator circuits are similar to those of the TC1180. In addition, the chip contains clock drivers for the CCD and the program registers. The two-phase, shallow buried channel CCD has double poly-Si gates. Other circuits are NMOS.



b. *Performance.* The upper photo shows the auto-correlation of a 128-bit biphase code (lower trace) at a 10-Mb/s data rate. The CCD is being operated here by the on-chip clock drivers. The reference code was loaded via the program register, which was driven by the on-chip clocks.

Fig. 2-3. Characteristics and performance of TC1221 self-contained 128-stage analog-binary correlator.

2.2 BASIC CORRELATION CIRCUITS

The correlation circuits, shown in Fig. 2-4, are required to accept and store a reference code, and then compare it to an incoming signal. The circuits and their functions are:

- Program register — a binary, serial-in/parallel-out shift register through which the binary reference code is loaded. To save loading time, the two 256-bit sections may be loaded in parallel.
- Binary latches — flip-flops constituting a static memory, in which the reference code is stored.
- Isolation switches — FETs connecting the program register to the binary latches. They control the parallel shift of data from the program register to the binary latches and, thus, permit the introduction of a new reference code into the program register while the correlator is still acting on the code previously stored.
- Routing switches — two FETs per CCD stage which steer the output of a given tap to the appropriate summing bus. The switches are controlled by the reference code stored in the binary latches.
- Tap and active load — two FETs per CCD stage which together with the routing switches convert the charge fluctuations on the CCD floating gate to tap voltage fluctuations. These voltage fluctuations are then averaged on the summing buses.
- CCD tapped delay line — two 256-stage, buried n-channel CCD registers coupled by a corner turning circuit (see Fig. 2-4).

The folded structure, indicated in Fig. 2-4, is used to facilitate packaging and optimize uniformity. The CCD has a low-noise input structure which samples the incoming signal and converts it to charge packets.

Figure 2-5 is a one-stage slice showing schematically all of the MOS devices, from the program register to the CCD register. Operation of these circuits is straightforward. The functions of the clocks shown in the figure are as follows:

- $\phi_{A'}$, ϕ_{B} — shift the reference code data through the program register
- ϕ_{ISO} — effects parallel transfer of the reference code from the program register to the binary latch
- ϕ_{RESET} — prepare the binary latch to receive data from the program register
- ϕ_{T} - transfer charge along the CCD register
- ϕ_{FG} — reset the floating gate to a DC reference, as often as once per sample interval.

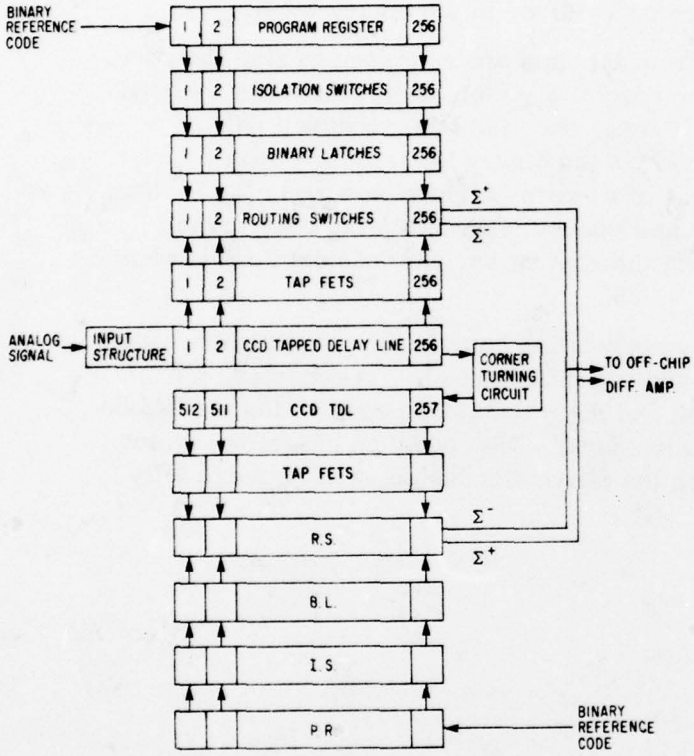


Fig. 2-4. Basic correlation circuits and correlator architecture.

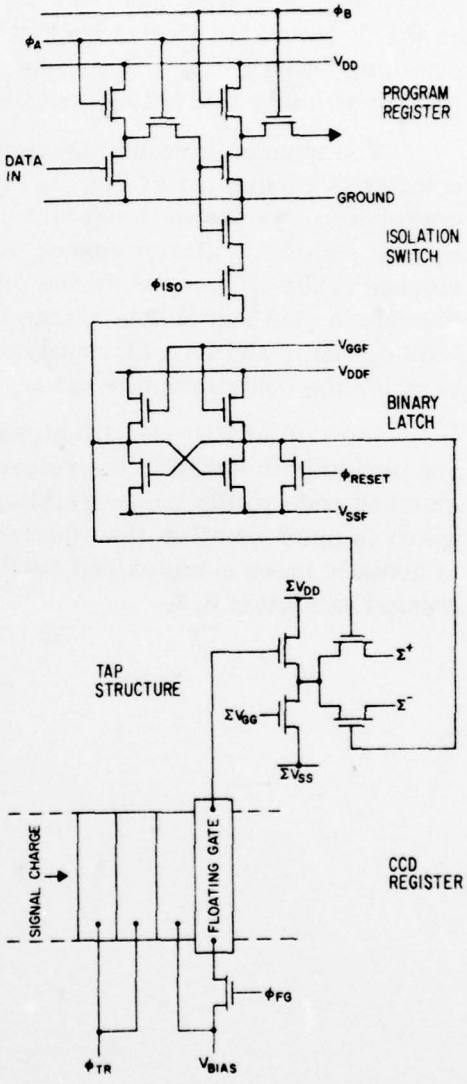


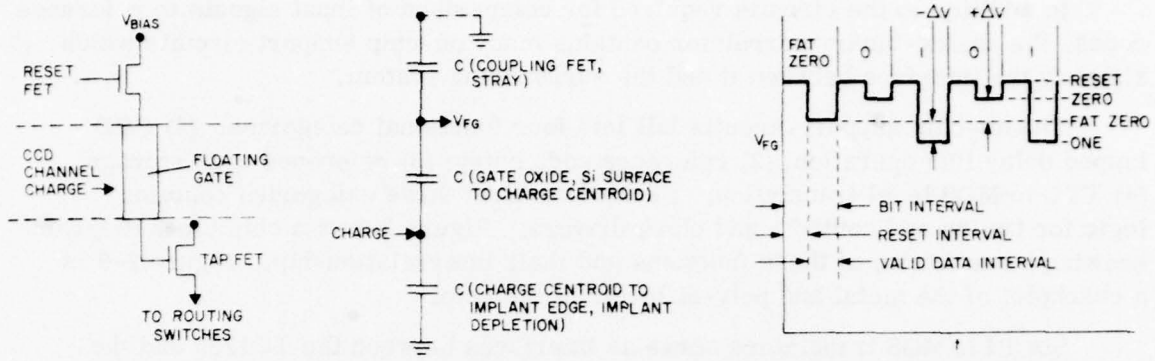
Fig. 2-5. One-stage slice through correlator.

2.3 CORRELATION WITH FLOATING GATE TAPS

Each floating gate tap (Fig. 2-6.a) nondestructively senses the signal charge as it propagates along the CCD channel. The floating gate is one of the CCD polysilicon gates. One end is connected to a dc bias via a switched transistor (hence the designation "floating gate"), while the other end is the gate of the tap FET (see Fig. 2-6.a). The signal charge propagating along the CCD channel will charge and discharge the capacitive network (Fig. 2-6.b) associated with the floating gate. The change in charge under the gate will cause a proportional voltage fluctuation on the floating gate electrode (Fig. 2-6.c). This fluctuation is coupled to one of the summing buses (Σ^+ or Σ^-) as determined by the status of the routing switches. The routing switches are set by the reference code stored in the binary latch.

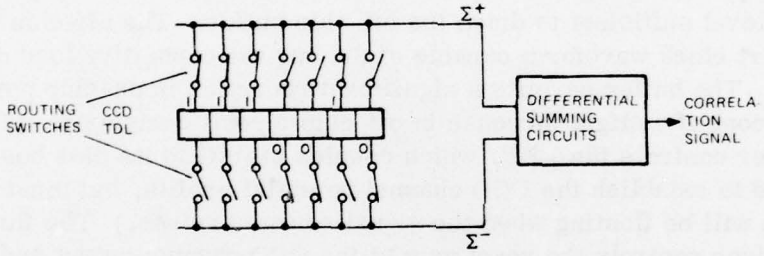
The manner in which the signals from the taps are combined to give the correlation is illustrated in Fig. 2-7 for the case of a simple seven-bit Barker-coded correlator. As shown in part (a) of the figure, each tap is served by a pair of routing switches. The presence of a "one" in the binary latch effects switch closure to the Σ^+ bus, while the presence of a "zero" effects closure to the Σ^- bus. Therefore, the signal determines the magnitude and sign of the tap contribution ($+\Delta V$ or $-\Delta V$), and the reference code (via the routing switches) determines the bus to which the contribution is made.

Part (b) of Fig. 2-7 illustrates the correlation outputs for two different codes: one perfectly matched to the reference and one mismatched. As expected, the matched code yields the correlation peak and the mismatched code yields a sidelobe which is much smaller than the correlation peak. The operation of the tap, which is actually more complex and subtle than the above discussion, will be more fully treated in Section 3.3.



(a) FLOATING GATE (b) CAPACITOR ARRAY (c) FLOATING GATE VOLTAGE WITH CODE BITS IN CCD REGISTER

Fig. 2-6. Signal charge sensing by floating gate tap.



(a) TAPPED DELAY LINE CONFIGURATION FOR RECOGNITION OF 7-BIT BARKER CODE: 1110010.

INPUT SIGNAL	CORRELATION SIGNAL
MATCHED: 1110010 CODE	CORRELATION = $\lvert \Sigma^+ - \Sigma^- \rvert$ = $\lvert 4(-\Delta V) - 3(+\Delta V) \rvert$ = 7 ΔV (I.E. CORRELATION PEAK)
UNMATCHED: 0101011 CODE	CORRELATION = $\lvert [2(-\Delta V) + 2(+\Delta V)] - [2(-\Delta V) + 1(+\Delta V)] \rvert$ = ΔV (i.e. UNITY SIDELOBE)

(b) CORRELATION OUTPUTS FOR DIFFERENT CODES

Fig. 2-7. Operation of a simple programmable correlator.

2.4 ON-CHIP SUPPORT CIRCUITS

In addition to the circuits required for comparison of input signals to reference codes, the analog-binary correlator contains many on-chip support circuits which simplify the interface between it and the surrounding system.

The on-chip support circuits fall into four functional categories: (1) CCD tapped delay line operation; (2) reference code entry; (3) reference code storage; (4) TTL-to-MOS level translation. Each of the first three categories contains logic for timing and control, and clock drivers. Figure 2-8 is a chip block diagram showing a breakdown of these functions and their interrelationship. Figure 2-9 is a checkplot of the metal and poly-Si levels of the chip.

Six TTL/MOS translators serve as interfaces between the TC1235 and the master oscillator, reference code generator, and load command generator. The translators shift the pulse amplitudes from the TTL level (4 V) to an MOS level of approximately 8 V (dependent on V_{DD}).

The CCD requires clock logic, a transport clock predriver, an input sampling circuit, a floating gate reset driver, and a floating diffusion reset driver. The clock logic circuit accepts an input from the master oscillator (via a TTL-to-MOS translator) and amplifies it for input to the CCD predriver. It also provides timing pulses for the input sampling circuit. The CCD predriver further amplifies the waveform to a level sufficient to drive the off-chip buffer. The off-chip buffer provides a transport clock waveform capable of driving the capacitive load of the CCD register gates. The buffer permits a significant reduction in on-chip power dissipation at the cost of a slight increase in off-chip circuit complexity. The floating gate reset driver controls the FET, which couples the FG to its bias bus. (The bias is required to establish the CCD channel potential profile, but must be removed so that the gate will be floating when the signal charge arrives.) The floating diffusion reset driver controls the reset gate at the CCD channel output and permits removal of signal charge which has propagated the length of the channel.

The input sampling circuit controls the low-noise, fill-and-spill inputting of signal charge into the CCD register. It generates the input sampling pulse (strobe) in synchronism with the CCD register transport clock.

The code entry section includes the program register clock logic and driver. It accepts a low level input from the master oscillator (via an off-chip divide-by-N circuit and on-chip TTL-to-MOS translator) and provides: (1) the higher level clocks required to run the program register, and (2) timing signals for the load logic.

The code storage circuits are: load logic, isolation switch driver and latch reset driver. Collectively, these circuits control the parallel transfer of the reference code from the program register (a dynamic shift register) to the binary latch (a static memory). The load logic circuit accepts inputs from the internal program register driver and the external load command generator. These circuits provide timed outputs, through drivers, to the isolation switches and the binary latch reset transistors.

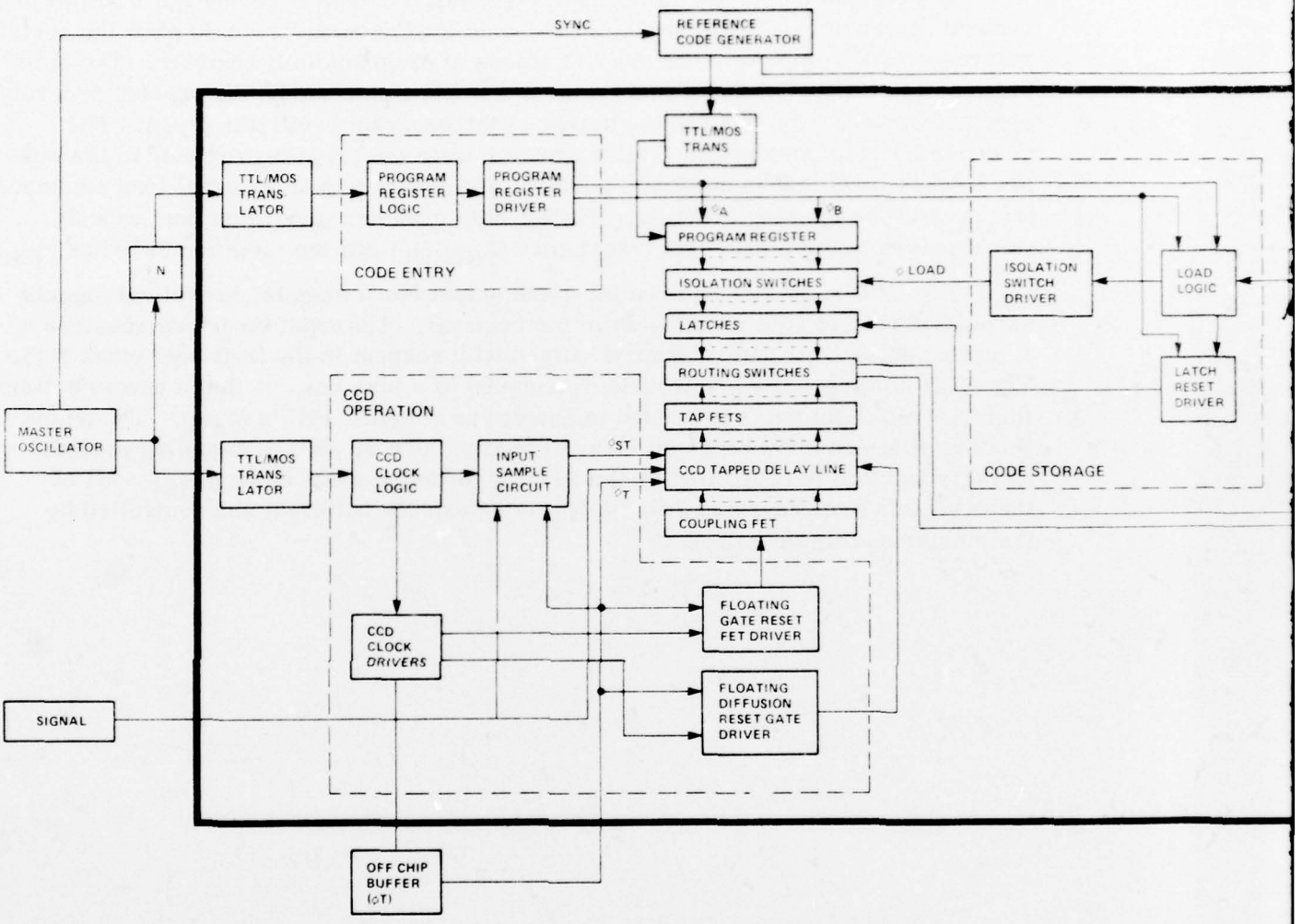
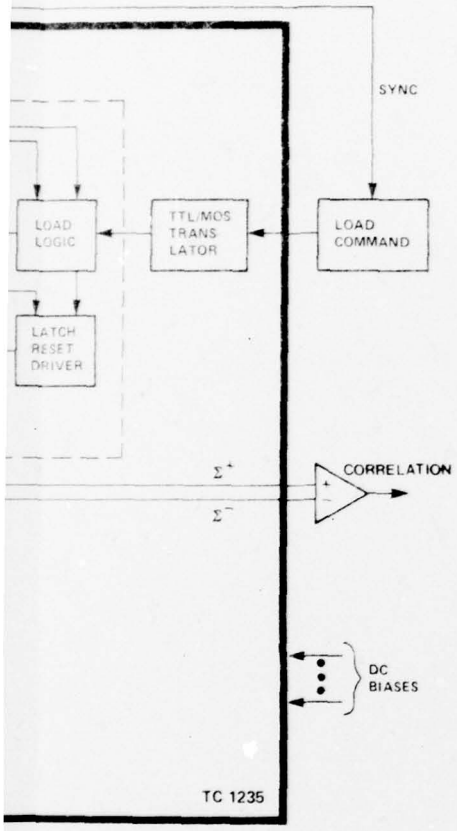
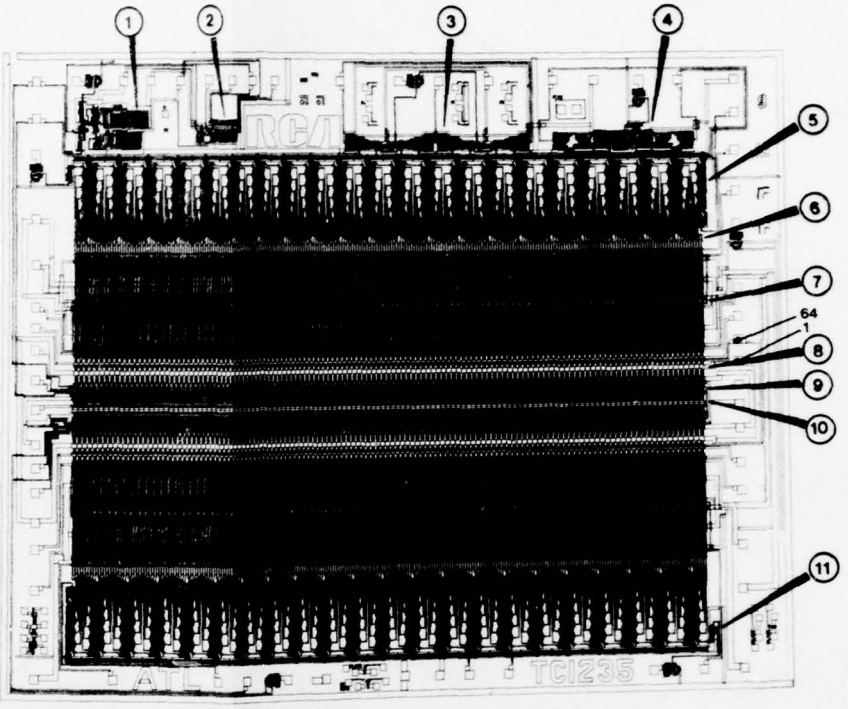


Fig. 2-8. TC1235 correlator chip, showing on-chip support circuits and off-chip interfaces.





1. CCD TRANSPORT CLOCK AND INPUT STROBE DRIVERS
2. FLOATING GATE AND FLOATING DIFFUSION RESET CLOCK DRIVERS
3. LOAD LOGIC
4. PROGRAM REGISTER DRIVER
5. PROGRAM REGISTER
6. ISOLATION SWITCHES
7. BINARY LATCHES
8. TAP FETS AND ROUTING SWITCHES
9. CCD TAPPED DELAY LINE
10. CORNER CIRCUIT
11. TTL TO MOS TRANSLATOR (TYPICAL)

Fig. 2-9. Metal and poly-Si levels of TC1235 correlator chip.

2

2.5 TIMING

The signals required to operate the TC1235 correlator are depicted in Fig. 2-10 and summarized in Fig. 2-11.

The signals employed in loading a code into the binary latches fall into two procedural categories. The first step in the code loading sequence is to shift the serial reference code completely into the 512 stages of program shift register. The shift register is clocked by the ϕ_A and ϕ_B clock signals generated by the on-chip program register driver. The input to the driver is the program oscillator (ϕ_{PO}). The second step is to perform a parallel transfer from the program register to the binary latches. All that is needed to perform this function is an external load command (ϕ_{LOAD}) to the load logic/driver. The on-chip circuitry generates the properly timed pulses to the latch reset transistors (ϕ_{RESET}) and the isolation switches (ϕ_{ISO}).

The CCD register requires input and output clock signals, as well as signals associated with charge transfer down the register. The input structure requires a sampling pulse (ϕ_{SI}) that is properly timed with respect to the transport clock (ϕ_T). The CCD floating gates are transistor-coupled to a bias bus, so that a properly timed floating gate reset pulse is needed to enable the coupling FET's (ϕ_{FG}). The output floating diffusion must be swept clear of charge between charge sampling periods, and this function is controlled by the floating diffusion reset clock (ϕ_{RG}). All of these signals are generated on-chip (ϕ_T is externally buffered) and controlled by the master oscillator (ϕ_{MO}).

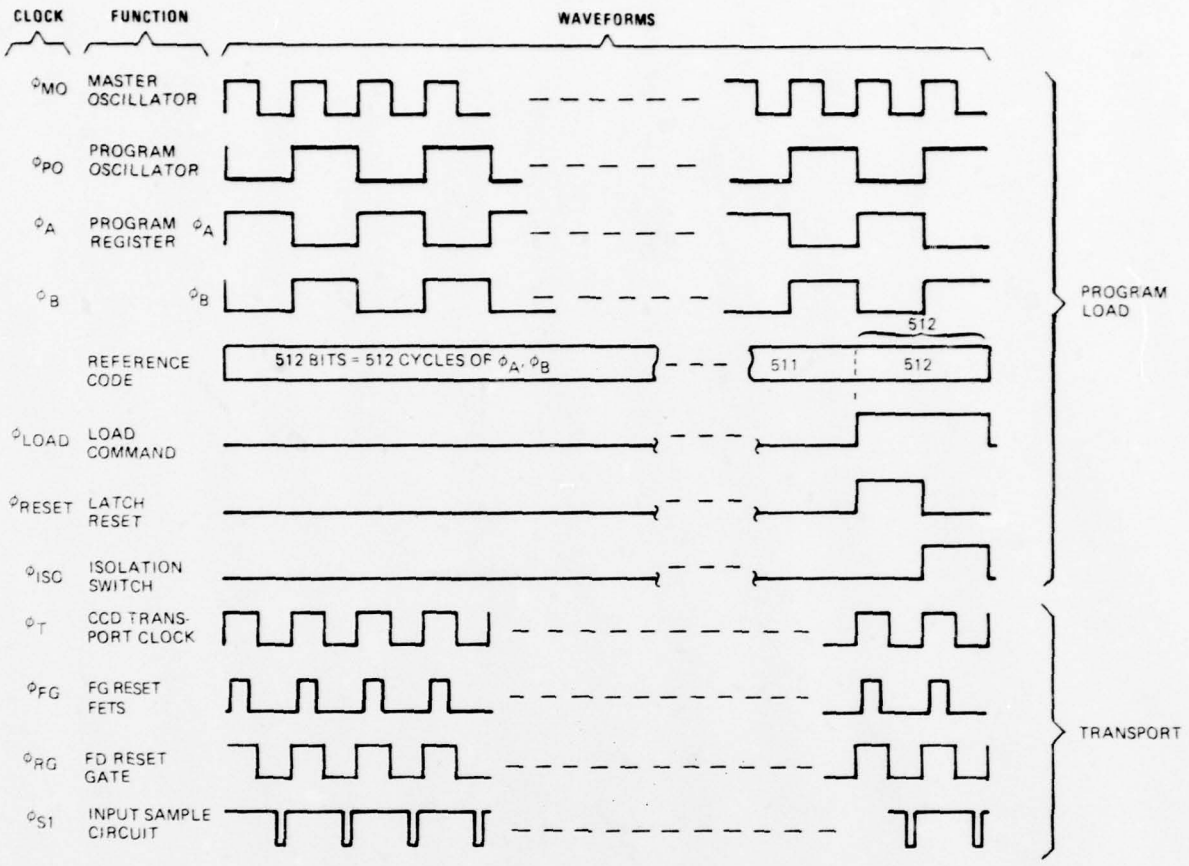


Fig. 2-10. Correlator timing and control signals.

ϕ_{MO} ----- 10 MHz, 50% DUTY

ϕ_A, ϕ_B --- 5 MHz, 50% DUTY

ϕ_T ----- 10 MHz, 50% DUTY

ϕ_{LOAD} --- 1 CODE BIT WIDE

ϕ_{FG} ----- 10 MHz, <50% DUTY

ϕ_{RG} ----- 10 MHz, 50% DUTY

ϕ_{S1} ----- 10 MHz, <<50% DUTY

ϕ_{RESET} -- IN SYNC WITH ϕ_A AND ϕ_{LOAD}

ϕ_{ISO} ---- IN SYNC WITH ϕ_B AND ϕ_{LOAD}

Fig. 2-11. Clock signal characteristics.

Section 3.0

DETAILED DESIGN
of
ANALOG-BINARY CORRELATOR

3.1 PROCESS TECHNOLOGY

The self-aligned-gate BCCD/NMOS process is a proven, RCA process. It produces CCD and MOSFET structures of the type shown in Fig. 3-1. The parasitic gate capacitance due to drain/source overlap is reduced by 70% compared to that obtained with the non-self-aligned process. This reduction in parasitic capacitance will increase the maximum operating frequency and reduce the per-stage power consumption of the TC1235, as compared to earlier correlator chips.

The mask levels used for the fabrication of the TC1235 are listed in Table 3-1, and the process flow chart is shown in Fig. 3-2. This is a double polysilicon gate process, with a barrier implant under the second level gates. Due to the barrier implant ($N_D = 3.5 \times 10^{11}$ cm^{-2}), the second polysilicon gate FET's are depletion devices with a threshold voltage $V_T \approx -8$ volts.* The first polysilicon gate FET's are enhancement devices with a threshold voltage $V_T \approx 0.9$ volt.*

The barrier implant creates a 4.0 volt decrease in the V_{MB}** potential under the second level gates in the CCD buried channel. This potential offset between second and first level CCD gates creates the necessary charge flow directionality for the pairs of transfer gates and the pairs of dc gates (one second level and one first level in each pair).

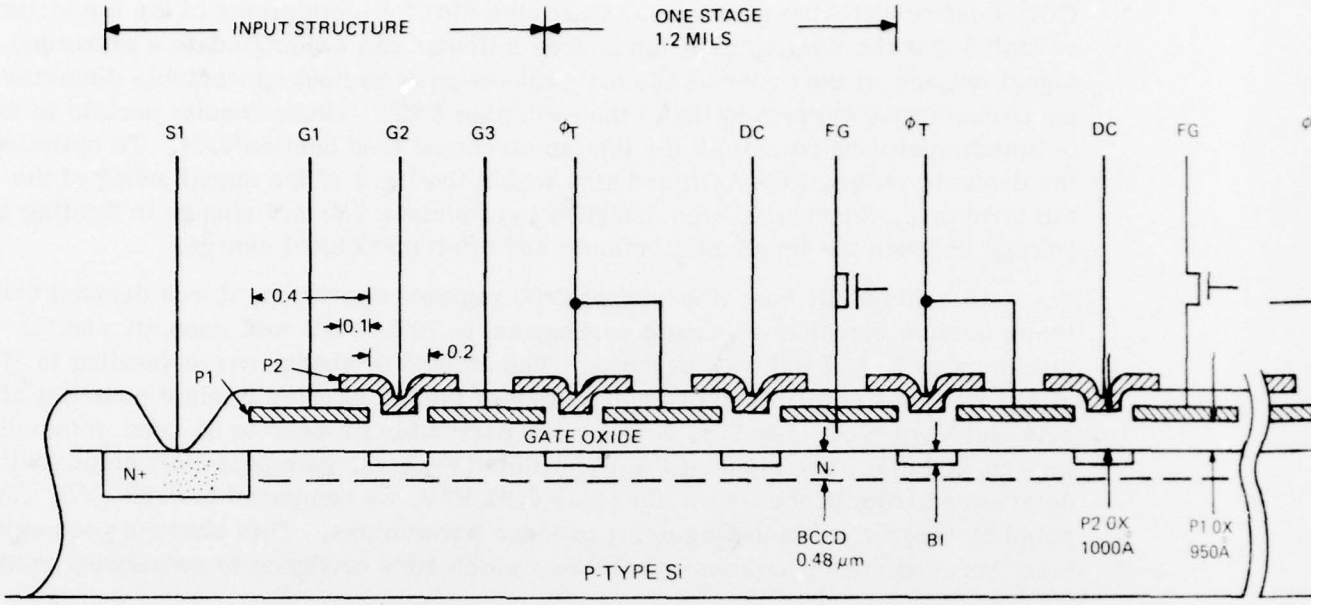
The shallow buried layer of the CCD channel has an effective profile depth of 0.48 μm, typically. Measurements on other devices fabricated with this process indicate that the transfer loss (ϵ) at a 1-MHz clock frequency will be between 1×10^{-5} and 2×10^{-5} per transfer. At a 10-MHz clock frequency, the transfer loss will be less than 5×10^{-5} per transfer. The CCD channel uniformity and noise characteristics have been very good on the devices measured. It is expected that the TC1235 performance will further substantiate the advantages of the self-aligned-gate BCCD/NMOS process.

TABLE 3-1. MASK LEVELS USED IN SELF-ALIGNED-GATE BURIED CHANNEL PROCESS

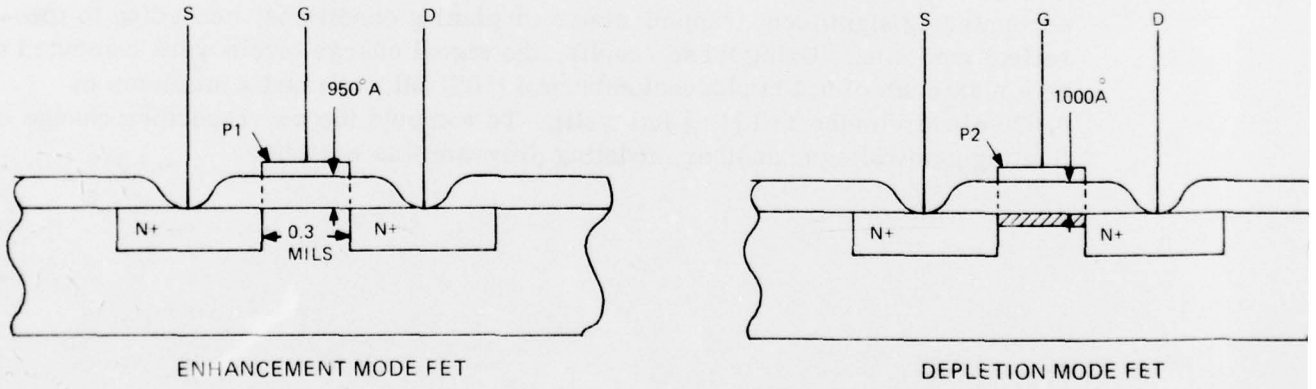
Mask Level	Description
M5	BCCD channel
M6	MOS channel
M9	Poly 1
M10	Poly 2
M11	Contacts
M12	Metal
M13	Pads

* Threshold voltage at zero-reverse-gate bias.

** V_{MB} is defined as the buried channel potential minimum with respect to the bulk (substrate) potential.

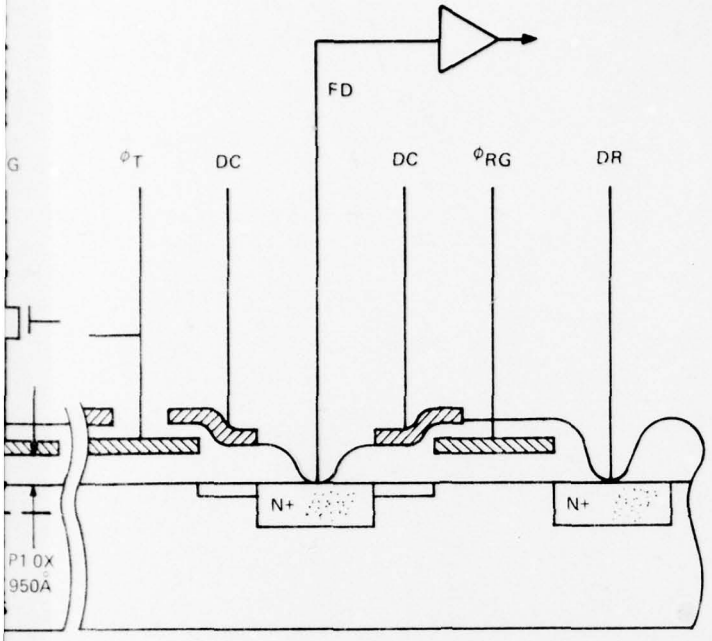


(a) BURIED CHANNEL CCD STRUCTURE



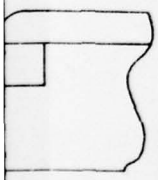
(b) SELF-ALIGNED MOSFET STRUCTURE

Fig. 3-1. Self-aligned-gate BCCD/NMOS process.



LEGEND

S1 – INPUT SOURCE
G1, G2, G3 – INPUT GATES
P1 – FIRST POLYSILICON GATES
P2 – SECOND POLYSILICON GATES
P1 0X – OXIDE THICKNESS UNDER P1
P2 0X – OXIDE THICKNESS UNDER P2
BCCD – BURIED CHANNEL IMPLANT
BI – BARRIER IMPLANT
ϕ_T – CLOCKED TRANSPORT GATES
DC – FIXED-BIASED GATES
FG – FLOATING GATES (TAPS)
FD – FLOATING DIFFUSION WITH CONNECTION TO OUTPUT AMPLIFIER
ϕ_{RG} – FLOATING DIFFUSION RESET GATE
DR – RESET DRAIN
HORIZONTAL DIMENSIONS IN MILS
VERTICAL DIMENSIONS NOT TO SCALE



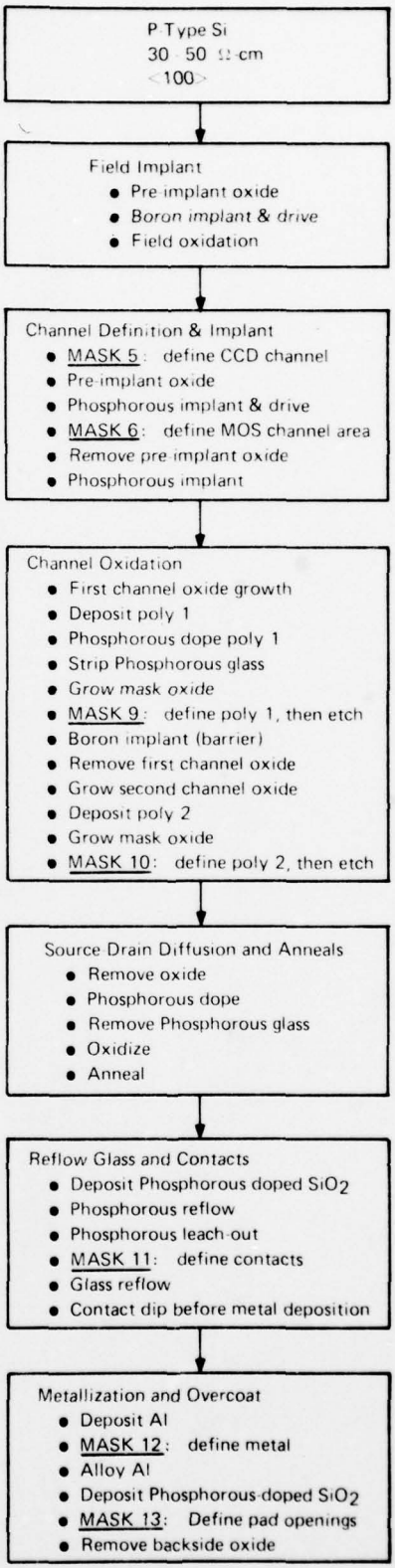


Fig. 3-2. BCCD/NMOS process flow chart.

3.2 CHARGE CAPACITY AND TRANSFER IN THE CCD CHANNEL

The CCD channel was designed to provide the maximum dynamic range for the CCD/floating-gate-tap structure. Extensive SPICE* simulations of the tap structure revealed that the floating gate/tap source follower can accommodate a maximum signal voltage of the order of 800 mV peak-to-peak without appreciable distortion appearing in the current swing of the switching FET. These results pertain to the optimum operating potentials for the tap structure (see Section 3.3). To optimize the dynamic range of the CCD and stay within the limit of the signal swing of the tap structure, the channel was designed to produce a 750-mV change in floating gate voltage between the levels of maximum and minimum signal charge.

To achieve the best linearity of CCD register operation, it was decided that the maximum signal level should correspond to 70% of full well capacity and the minimum to 10% of full well capacity. The amount of charge corresponding to 70% of full well was determined by examination of typical barrier implant potential offsets and V_{MB} plots (see Fig. 3-3) for the particular process to be used in fabricating the TC1235. The slope of the V_{MB} plots (V_{MB} vs. gate potential) empirically determined from processed wafers was 0.91 V/V, as compared to 0.895 V/V computed by theoretical modeling using process parameters. This shows a good agreement between theory and empirical data, which adds credence to subsequent modeling.

Figure 3-3 shows V_{MB} plots for the two polysilicon gates. Note that the poly-2 gates have implanted barriers beneath them, which lowers V_{MB} by 4 volts. With the V_{MB} plots and the estimated operating potentials contained in Table 3-6, one can construct a typical operating potential profile for the CCD register (as shown in Fig. 3-4).

The amount of charge corresponding to full well capacity, for a 4-volt V_{MB} barrier implant, was computed to be 0.198 picocoulombs/mil of channel width, for a register with 0.4-mil storage gates. This amount of charge can be accommodated with a great degree of latitude in register operating potentials without encountering significant trapping states or pinning conditions, according to theoretical modeling. Using these results, the signal charge levels were computed to be a maximum of 0.139 picocoulombs/mil (70% full well) and a minimum of 0.020 picocoulombs/mil (10% full well). To compute the corresponding change in floating gate voltage, another modeling program was written.

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* SPICE is a circuit analysis program developed at the University of California, Berkeley, and now used widely, especially where harmonic analysis is required. It was the primary simulation tool for analysis of the tap structure.

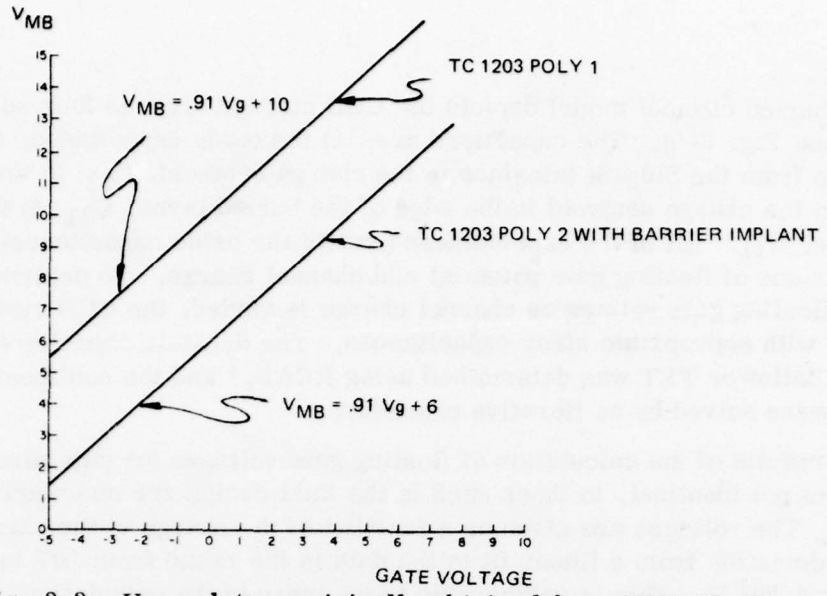
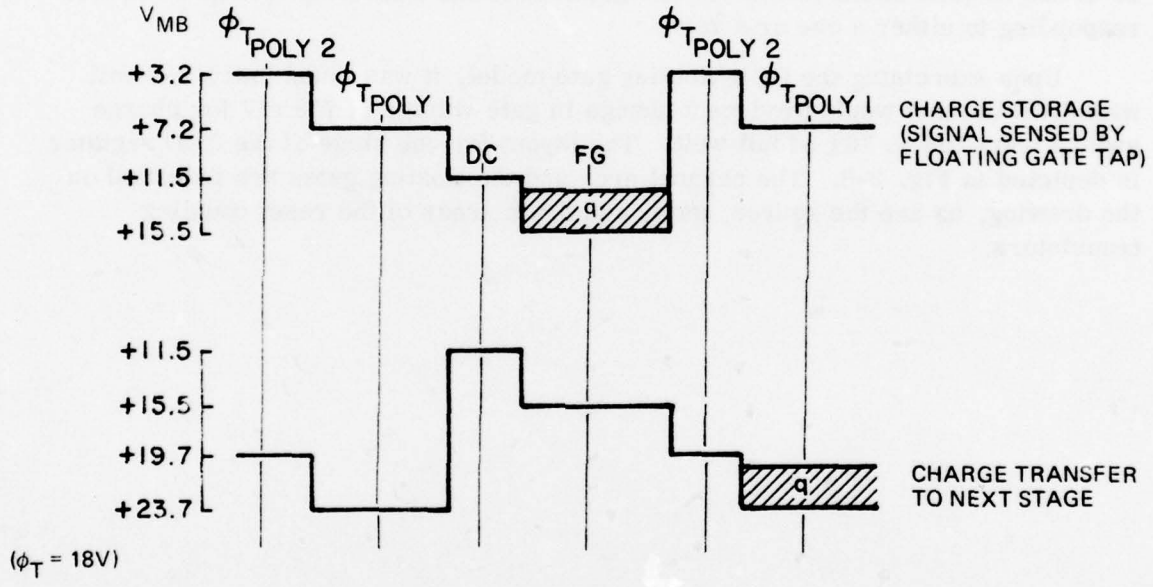


Fig. 3-3. V_{MB} plots empirically obtained from TC1235 chips.



TYPICAL CLOCK AMPLITUDE AND BIAS LEVELS

ϕ_T : 18V AMPLITUDE; -3 TO +15V

DC : +6V

FG : RESET TO +6V PRIOR TO ARRIVAL OF SIGNAL CHARGE

Fig. 3-4. Potential profile.

The buried channel model depicts the CCD storage area as four series capacitors (see Fig. 3-5). The capacitors are: 1) the oxide capacitance, C_{ox}; 2) the capacitance from the SiO_2-Si interface to the charge centroid, C_{22}; 3) the capacitance from the charge centroid to the edge of the buried layer, C_{21}; 4) the depletion capacitance, C_{11}. All of the capacitances (except the oxide capacitance) are nonlinear functions of floating gate potential and channel charge. To determine the change in floating gate voltage as channel charge is varied, the CCD model was augmented with appropriate stray capacitances. The dynamic capacitance of the tap source follower FET was determined using RCAP,* and the nonlinear model equations were solved by an iterative procedure.

The results of the calculation of floating gate voltages for gate dimensions similar, but not identical, to those used in the final design are summarized in Table 3-2. The voltages are given as a function of the charge in the channel. The maximum deviation from a linear fit to the data in the range from 10% to 70% of a full well is 0.001 V. This is comparable to an error in the calculation, so that firm conclusions regarding linearity can not be drawn. Still, we note that the deviation is quite small (about 0.3%) compared to the maximum voltage swing corresponding to either a one or a zero.

Upon exercising the CCD/floating gate model, it was found that a 2.2-mil wide CCD channel would produce a change in gate voltage of 753 mV for charge swings from 10% to 70% of full well. The layout for one stage of the CCD register is depicted in Fig. 3-6. The channel area and the floating gates are indicated on the drawing, as are the source, gate, and drain areas of the reset coupling transistors.

* RCAP is an RCA circuit analysis program. It was used to corroborate the SPICE results in tap design and to analyze all other circuits.

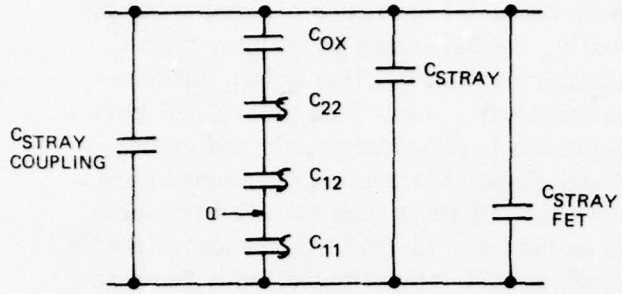


Fig. 3-5. CCD storage area as depicted by buried channel model.

TABLE 3-2. FLOATING GATE VOLTAGES AS A FUNCTION OF CHANNEL CHARGE

Q/Q_{FULL}	V_{FG1} (1) (Volts)	V_{FG2} (2) (Volts)	$V_{FG2} - V_{FG1}$
0.0	6.000	6.002	+0.002
0.1	5.894	5.895	+0.001
0.2	5.788	5.788	0.000
0.3	5.681	5.680	-0.001
0.4	5.573	5.573	0.000
0.5	5.465	5.466	+0.001
0.6	5.358	5.358	0.000
0.7	5.250	5.251	+0.001
0.8	5.141	5.144	+0.003
0.9	5.033	5.037	+0.004

(1) These values were computed from the circuit equations.
(2) These values were computed from the slope-intercept formula. with the slope determined by the V_{FG1} values for $Q/Q_F = 0.1$ and 0.7 and the intercept determined by the slope and V_{FG1} at $Q/Q_F = 0.4$.

slope = -1.073 volts/full well
intercept = 6.002 volts.

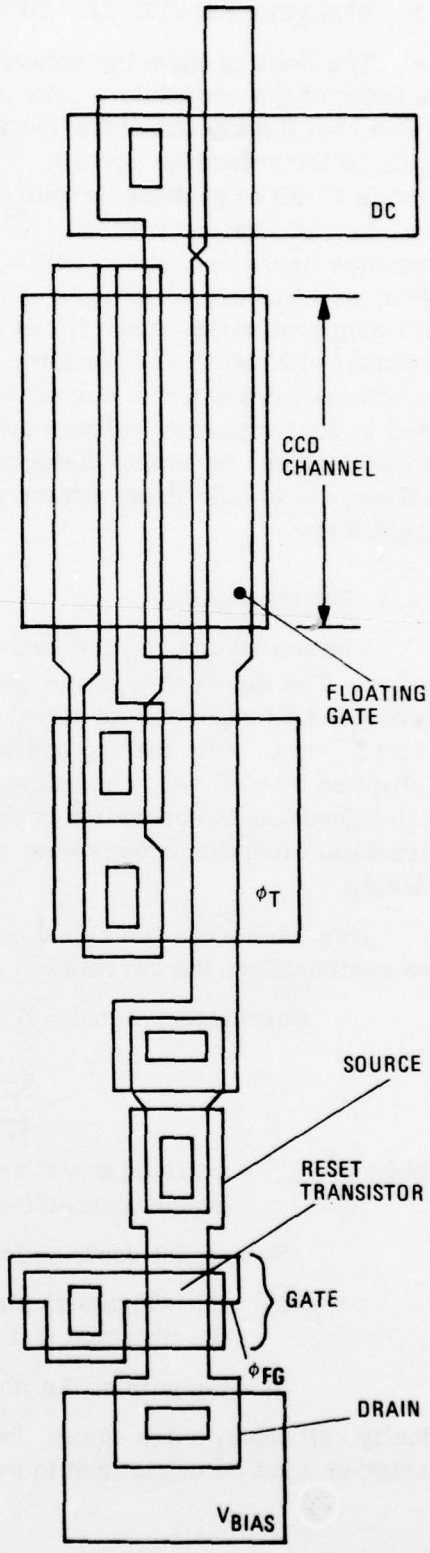


Fig. 3-6. CCD register stage layout.

3.3 FLOATING-GATE-TAP DESIGN

The floating-gate-tap structure, consisting of four FETs per CCD stage, is the heart of the correlator. The other circuits are important in operating the device, but the tap structure is where the fundamental operation of comparing the signal to the reference occurs. Theoretically, the 512-stage correlator should provide 27 dB of processing gain and an autocorrelation function with a peak-to-sidelobe ratio determined only by the code structure. Less than theoretical performance by the correlator will cause a decrease in processing gain and could nullify some of the advantages of the CCD approach. We are not concerned here with temporal noise, since it has been shown that CCDs in general are low-noise devices, with the CCD correlator being no exception. Instead, the concern is with the effects related to the correlator architecture and, specifically, with those related to the large size and high density of the correlator. The effects are: code dependent bias, harmonic distortion, and tap-to-tap nonuniformity. The design challenge is to hold these effects at tolerable levels while keeping tap power dissipation low.

3.3.1 Tap Operation

The tap structure produces the multiplication function at each stage of the device. The signal charge is linearly sensed by the floating-gate-tap source follower, and a proportionate signal is coupled via the routing switches to either the Σ^+ or Σ^- bus. This routing operation, in effect, creates the product of the signal multiplied by +1 or -1, depending upon the reference code stored in the latch. (Latch function and operation is described in Section 3.13.) The completion of the correlation function occurs when the summation lines are differentially summed off-chip.

At a time when the signal completely fills the correlator, so that all stages are contributing, the correlation peak signal is given by:

$$\text{Correlation Signal} = \Sigma^+ - \Sigma^-$$

$$= \sum_{j=1}^{512} \alpha_j \left[W_j S_j - \overline{W}_j S_j\right]$$

where Σ^+, Σ^- = summed contributions of all taps connected to Σ^+ and Σ^- buses, respectively.

S_j = signal contribution at the jth stage.

W_j, $\overline{W}_j$ = tap weights at the jth stage. (If the reference code at the jth stage is 1, then $W_j = 1$ and $\overline{W}_j = 0$, and vice-versa.)

α_j = tap gain at the jth stage.

Ideally, all the α_j's are equal. In practice they may vary over the array and this variation must be minimized to avoid degradation in the correlation.

3.3.2 Tap Circuit and Code-Dependent Bias

The tap structure[3] consists of: 1) a source follower FET with the gate floating over the CCD channel; 2) an active load FET; 3) two routing switch FETs. The source follower and active load FETs are biased in saturation. Together they produce a replication of the floating gate voltage at the common node (see Fig. 3-7). This voltage swing at the common node is coupled to one of the summing buses by the latch-enabled switch FET.

This tap configuration ensures that there is no code-dependent bias[4] product present in the correlation signal. Earlier correlator designs, in which the tap structure lacked the active load device, did exhibit code-dependent bias. This problem manifests itself as a large dc offset in the correlation. The offset is different for codes with different ratios of ones and zeros. It may be adjusted out for any given code, but it returns whenever the code balance is changed. In the present design if there is no signal, i.e., no charge differing from fat-zero, under the floating gate of a given stage there will be no contribution by that stage to the Σ^+ or Σ^- bus during the valid correlation interval of each clock period.

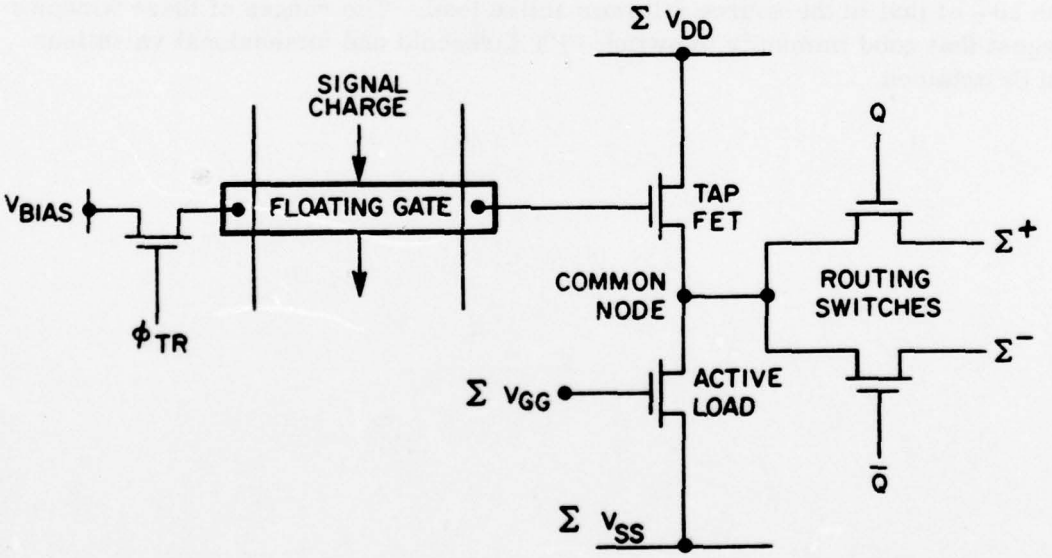


Fig. 3-7. Details of the floating gate tap structure.

3.3.3 Harmonic Distortion and Power Dissipation

Simulation using SPICE and RCAP led to a tap structure design with large dynamic range, large bandwidth, low distortion and low power dissipation. The design goal was 500 mW, or less than 1 mW per tap. With the ΣV_{DD} voltage restricted to the 6 to 7 volt range due to CCD register constraints, the current level in the tap source follower is limited to a maximum of approximately 150-160 μA.

Because of the low quiescent current in the unloaded source follower, even small currents deviated from the active load to the switch FET can increase distortion in the source follower. However, analysis and SPICE simulation indicate that it is possible to select FET dimensions and biases which will cause the current through the switch FET to have a much lower distortion than the voltage on the common node which drives it. The result is a linear transfer function between the floating gate voltage and the switch FET current.

The calculated distortion of the tap structure is indicated in Fig. 3-8. Total harmonic distortion (THD) and peak signal current are plotted against switch FET gate voltage. The SPICE results are for a single tap with 800 mV peak-to-peak sinewave (corresponding to the largest expected signal) applied to the floating gate node, and the active summation bus appropriately biased.

The curve shows a minimum in THD as a function of switch FET gate voltage. Within a 1-volt window (e.g., 7.7 to 8.7 V) THD of 0.40% can be obtained, while within a 0.5-volt window (e.g., 7.9 to 8.4 V) 0.20% THD is possible. This performance is possible even though the peak current in the switch FET is more than 20% of that in the source follower active load. The ranges of these windows suggest that good immunity to switch FET threshold and dimensional variations can be obtained.

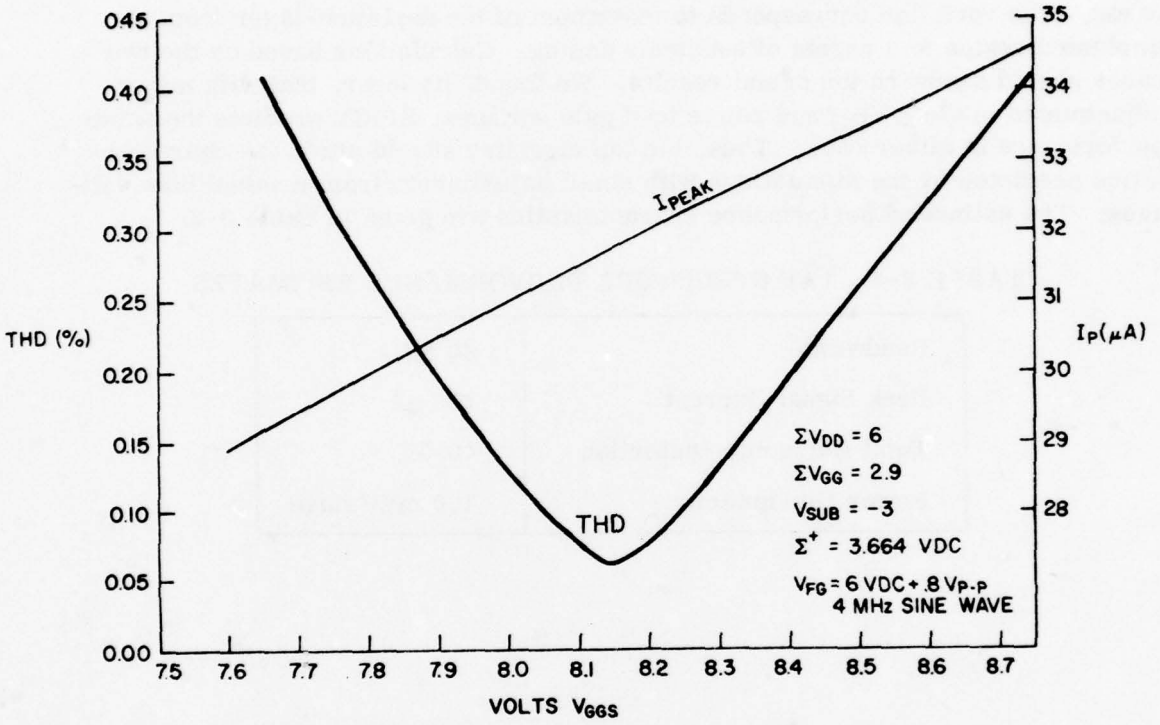


Fig. 3-8. Harmonic distortion in the tap structures as a function of routing switch gate voltage.

3.3.4 Process Parameter Variations

Further simulations predicted tap performance over the range of process parameter variations. The major variant from process run to process run is the ion implant level in the enhancement NMOS channels. Since the SPICE model has no provisions to accommodate a channel ion implant, the simulation was done with two values of uniform substrate doping. The first corresponded to the largest implant dose in the channel implant profile, the second to the actual substrate doping. Threshold voltage as a function of back gate bias is expected to differ in the two cases. The variation corresponds to movement of the depletion-layer from an implanted region to a region of substrate doping. Calculations based on the two cases should sandwich the actual results. We found, however, that with minor adjustments in the ΣV_{DD} and active load gate voltages, SPICE predicts the same performance in either case. Thus, the tap circuitry should attain the characteristics predicted by the simulations with small adjustments from nominal bias voltages. The estimated performance characteristics are given in Table 3-3.

TABLE 3-3. TAP STRUCTURE PERFORMANCE ESTIMATES

Bandwidth	40 MHz
Peak Signal Current	±30 μA
Total Harmonic Distortion	<0.5%
Power Dissipation	1.0 mW/stage

3.3.5 FET Dimensional Variation

The design for the tap structure considered not only process parameter variations, but also FET dimensional variations caused by photomask nonuniformity, photomask misalignment and process geometry variations. Large FET dimensions diminish the impact of registration errors and photomask runout effects, but are inconsistent with the goals of low power dissipation and high operating frequency. Implementation of moderately large FETs, together with the use of electron beam lithography in photomask fabrication, is an attractive compromise.

Electron beam lithography is superior to the conventional photo-optical technique. It results in masks which give better device performance as well as better yield. The Manufacturing Electron Beam Exposure System (MEBES) produces photomasters directly from magnetic tapes, eliminating several steps, each of which results in some error. MEBES mask production is not subject to the usual optical distortions, resulting in positional accuracy and line size uniformity an order of magnitude better than those obtained with conventional photolithography. Empirically, it appears that the defect density in the MEBES masks is lower than in conventionally produced masks. This, coupled with the superior alignment properties (associated with the greater precision), should result in higher fabrication yield, as well as greater tap uniformity.

The self-aligned silicon gate process also contributes to dimensional uniformity. The N^+ diffusions and gate regions are defined by two masks, the MOS channel/thin oxide mask and the first polysilicon mask. The channel length, gate-to-drain overlap and gate-to-source overlap are defined by a single mask. The channel width is defined by the MOS mask alone, since it defines the area for the channel implant and the field oxide step. This method of FET definition greatly reduces the effects of mask-to-mask misalignment as compared to the non-self-aligned processes.

A minor process modification contributing to greater uniformity is the use of thicker metalization. This modification is necessary because the resistance of the standard Al buses would result in significant voltage drops along the ΣV_{DD} and ΣV_{SS} buses. The voltage gradient along the ΣV_{SS} bus is especially important, because it affects the $(\Sigma V_{GG} - \Sigma V_{SS} - V_T)$ quantity in the current expression for the tap active load. To minimize voltage gradients along these buses, the Al deposition for the TC1235 will be 24,000 Å, twice that usually employed. This, and the large metal line widths and multiple bonding pads employed on either side of the array, should lead to the tap-to-tap uniformity required of the correlator.

3.4 CORNER DIFFUSION

The TC1235 was designed in a folded configuration in order to achieve a better aspect ratio. The correlator is divided after the 256th stage. Continuity is achieved between the 256th and 257th stages by a corner diffusion.[5]

The corner diffusion and the associated gate structure are shown in Fig. 3-9. The corner diffusion consists of two N^+ diffusions connected by an aluminum bus. The actual register division occurs in the middle of the second polysilicon clocked transfer gate (ϕ_{T21} and ϕ_{T22}) of the 257th stage. Because of the adjacent first polysilicon gate overlaps and the 0.05-mil lateral diffusion of the N^+ diffusions in the buried channel, the effective gate length of this transfer gate structure is 0.5 mil, only 25% greater than that of the first polysilicon storage gates.

The operation of the corner diffusion mechanism can be understood by referring to Fig. 3-10. When ϕ_T goes high, the potential well under the ϕ_{T21} gate accepts charge from the floating gate well of the 256th stage. The charge flows into the floating diffusion structure, is spilled into the well under the ϕ_{T22} gate, and is finally received by the first polysilicon transfer well of the 257th stage (ϕ_{T11} gate). This mode of operation is a modified bucket brigade, incomplete charge transfer operation.

The corner diffusion and the ϕ_{T22} and ϕ_{T11} gates, taken together, can be modeled as an FET. The depletion potential of ϕ_{T11} is the effective drain, ϕ_{T22} is the gate, and the corner diffusion is the source. The FET is biased as a source follower, with the corner diffusion capacitance as its load. Under these conditions the charge remaining on the diffusion after a transfer period is:

$$Q_r = Q_o \left[1 + \frac{\beta Q_o}{4 f_c C_{CD}^2} \right]^{-1}$$

where Q_o is the initial charge. If the device is operated with a fat zero (Q_b) and a signal charge (Q_s), then $Q_o = Q_b + Q_s$, and the transfer inefficiency for the corner stage is given by:

$$\epsilon_{corner} = \frac{dQ_r}{dQ_s} = \left[1 + \frac{\beta (Q_b + Q_s)}{4 f_c C_{CD}^2} \right]^{-2}$$

where Q_r is the charge remaining, f_c is the CCD clock frequency, C_{CD} is the corner diffusion capacitance, and β is the FET gain factor, $W\mu C_i/L$. Here, W and L are the FET channel width and length, μ is the electron mobility, and C is the channel capacitance. Measurements on devices processed using RCA's BCCD process yield a typical μC_i value of 13.5×10^{-6} A/V^2. The upper limit on the equation occurs at the lowest value for $Q_b + Q_s$. The lower operating limit for the CCD register may be taken as 10% full well capacity ($Q = 0.440 \times 10^{-13}$ coul.). Using this charge value for $Q_b + Q_s$, $f_c = 10$ MHz, $C_{CD} = 0.091$ pf, and ϵ (corner-max) = 0.007. Thus, the corner does not have an adverse impact on device performance.

Fig. 3-9. Structure of corner diffusion and associated gate.

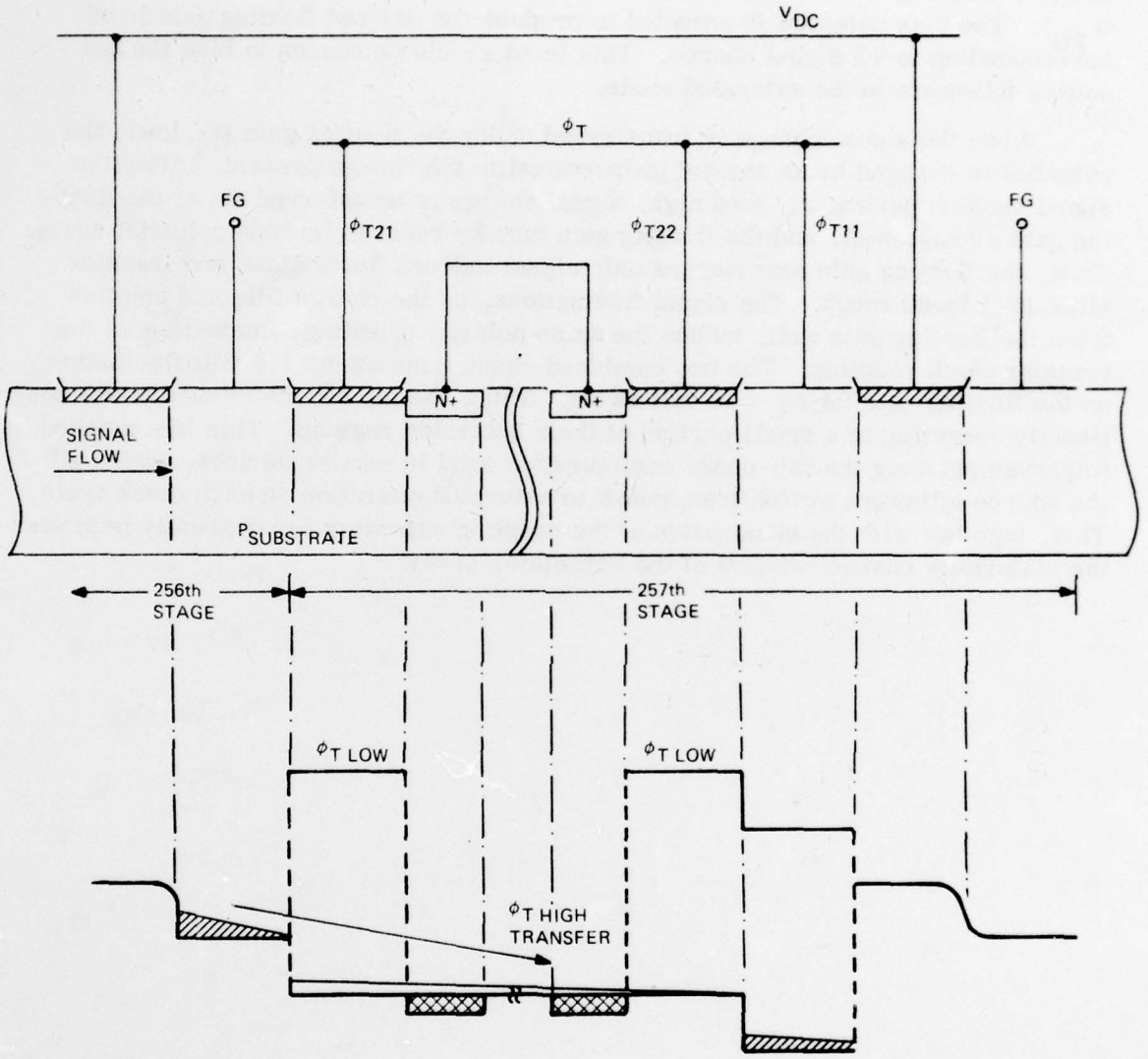


Fig. 3-10. Operation of corner diffusion.

3.5 UNIPHASE CLOCKING

Uniphase clocking of the CCD register enhances the operating characteristics of the floating gate tap. In the uniphase configuration, the floating gate is not clocked with a large transfer clock ($\approx$8 volts) as in two-phase operation (see Fig. 3-11). Instead, the floating gate is reset to a dc bias potential during the transfer period (ϕ_T high) (see Fig. 3-12). The reset action is accomplished by use of a coupling transistor, which is clocked by the floating gate reset clock (ϕ_{FG}). The bias potential is adjusted to produce the desired floating gate level corresponding to 0% signal charge. This level should be chosen to bias the tap source followers in the saturated mode.

When the signal charge is transferred under the floating gate (ϕ_T low), the potential is changed by an amount proportional to the charge present. After the signal sensing period, ϕ_T goes high, signal charge is transferred out of the floating gate storage well, and the floating gate may be reset to its bias potential again. Thus, the floating gate experiences only signal induced fluctuations and transfer clock (ϕ_T) feedthrough. The signal fluctuations, as the charge fills and empties from the floating gate well, induce the same polarity of voltage fluctuation as the transfer clock coupling. The two combined cause a maximum 1.8 volt fluctuation on the floating gate for ϕ_T = 18 volt swing. Thus, the tap source followers are continually operating in a small portion of their saturated regions. This is a marked improvement over the two-phase configuration used in earlier devices, where all the source followers switch from cutoff to saturated operation on each clock cycle. This, together with the elimination of the coupling capacitor array greatly improves the uniformity characteristics of the correlator array.

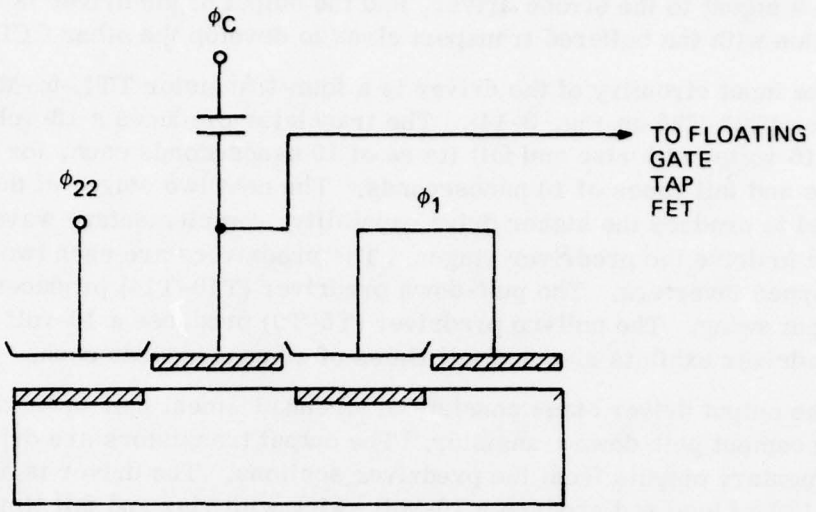


Fig. 3-11. One stage of two-phase structure with barrier implants.

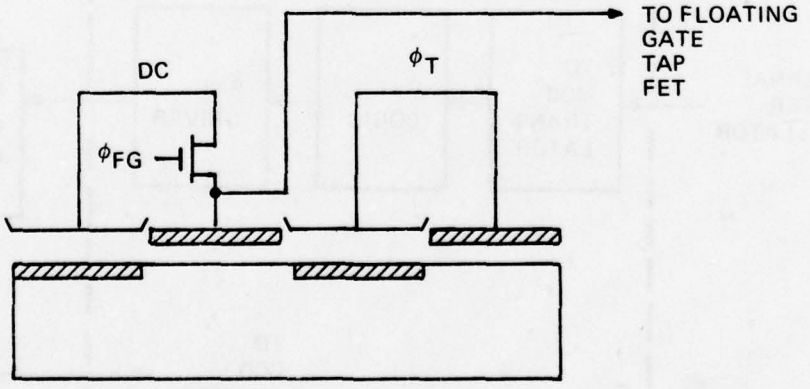


Fig. 3-12. One stage of uniphase structure with barrier implants.

3.6 CCD TRANSPORT CLOCK AND DRIVER

The CCD transport clock is developed on-chip to ensure proper timing of related clocking waveforms, then buffered and clamped off-chip in order to reduce on-chip power dissipation (see Fig. 3-13). The logic section of the transport clock driver supplies a signal to the strobe driver, and the output of the driver is used in conjunction with the buffered transport clock to develop the other CCD clock signals.

The input circuitry of the driver is a four-transistor TTL-to-MOS level translator (T23-T26 on Fig. 3-14). The translator produces a 13-volt swing (V_{DD} = 16 volts) with rise and fall times of 10 nanoseconds each, for a TTL input with rise and fall times of 10 nanoseconds. The next two stages of the driver are employed to produce the higher drive capability, complementary waveforms required to drive the predriver stages. The predrivers are each two-stage, bootstrapped inverters. The pull-down predriver (T10-T14) produces a 12.5-volt output swing. The pull-up predriver (T5-T9) produces a 16-volt output swing. This predriver exhibits rise and fall times of 10 nanoseconds each.

The output driver stage consists of an enhancement pull-up transistor and an enhancement pull-down transistor. The output transistors are driven by the complementary outputs from the predriver sections. The driver is designed to drive a 130-pf load and produce a 10-volt swing with rise and fall times of 20 nanoseconds each. This drive capability is more than sufficient to drive the intended bipolar buffer.

The buffer has been breadboarded and tested with the TC1221 ϕ_C driver as an input. The TC1221 ϕ_C driver has a slightly smaller drive capability than the TC1235 on-chip ϕ_T driver. With the buffer loaded at the ϕ_T design load of 220-pf (CCD gate capacitance plus package capacitance) a good 20-volt clock waveform was attained at a 10-MHz rate.

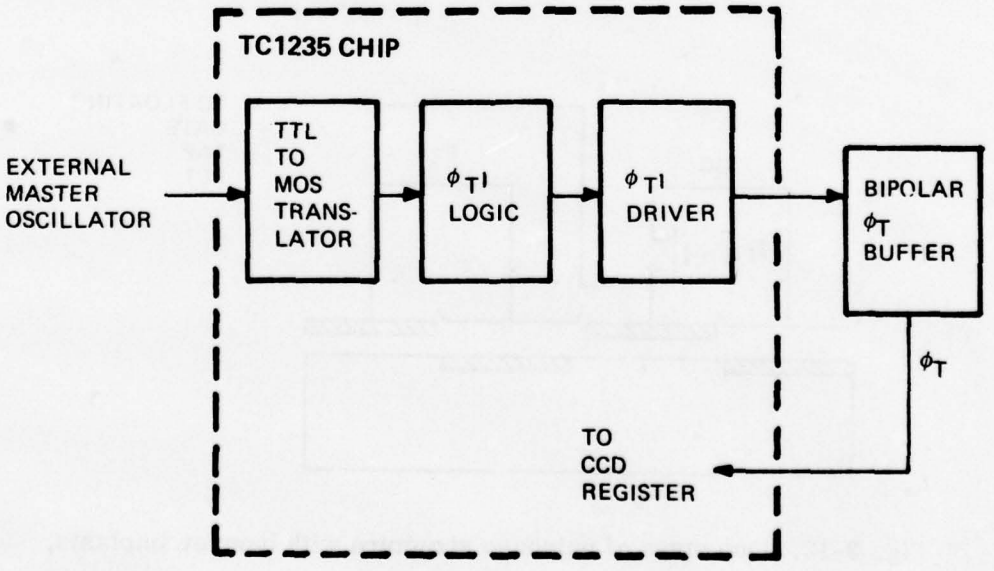


Fig. 3-13. CCD clocking process.

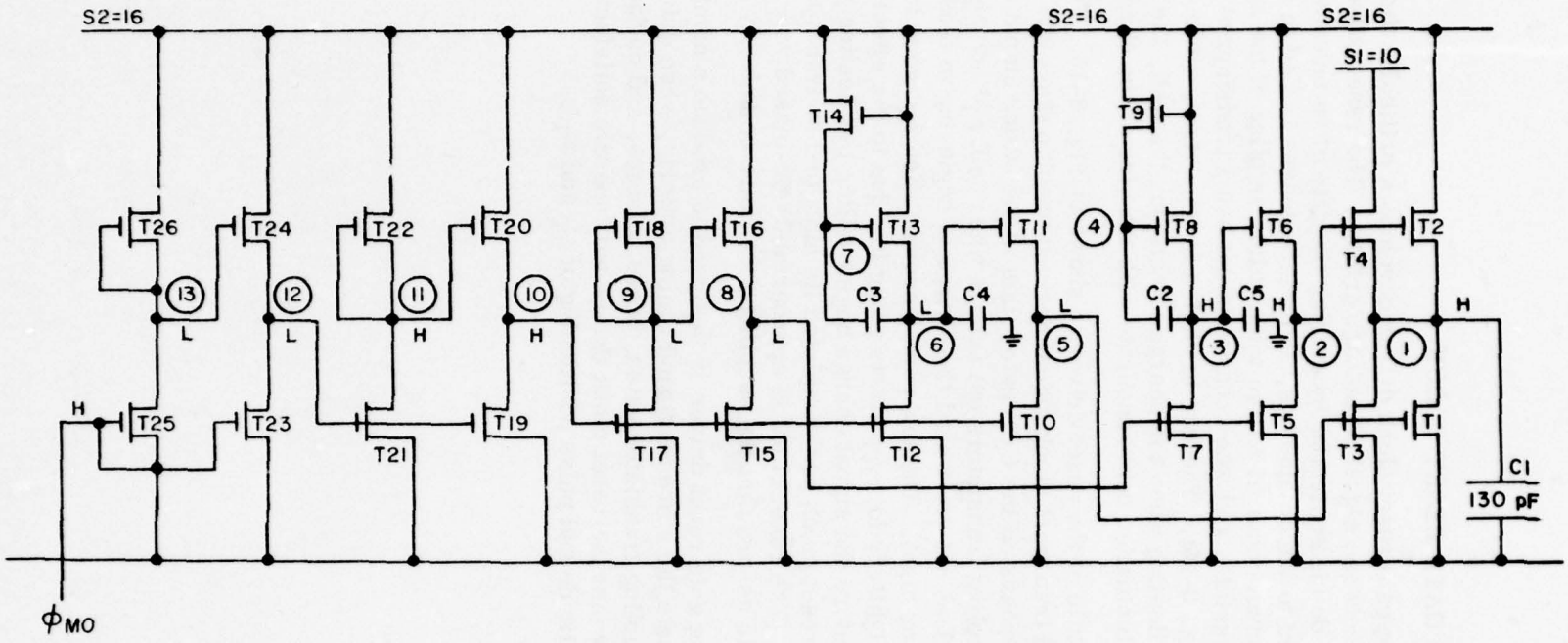


Fig. 3-14. Transport clock driver (ϕ_T') circuit.

3.7 FLOATING GATE RESET CLOCK

The floating gate reset clock driver develops a critically timed pulse to reset the floating gate between signal sampling periods. The reset pulse resets each floating gate to a dc bias potential by driving the gate of an enhancement FET, whose drain is connected to the dc bias bus, and whose source is tied to a floating gate. The reset pulse must occur at a time when valid sampling of the signal by the floating gate is not possible, and when charge is not being transferred into the floating gate well (see Fig. 3-15). The last criterion is important, since if the floating gate is not truly floating when the charge is entering the well, the charge will not cause a voltage fluctuation commensurate with the size of the charge packet.

The schematic of the reset driver is shown in Fig. 3-16. There are two inputs to the driver; the transport clock signal derived on-chip (ϕ_T') and the transport clock waveform that appears on the CCD gates (this is the buffer output (ϕ_T)). The high clock period (coupling transistors on) occurs when both ϕ_T' and ϕ_T are high. Thus, the reset action does not start until the charge is beginning to leave the floating gate well (ϕ_T going high). The low period occurs when ϕ_T' goes low. This transistion occurs slightly before ϕ_T starts going low due to the effective delay of the buffer. Thus, before the signal charge begins filling the floating gate well (ϕ_T at mid swing), the reset clock has completed its high-to-low transition and the floating gate is floating. (The reset clock is appropriately dc-biased with respect to the V_{BIAS} potential to assure that the coupling FETs turn completely on and off.)

The floating gate reset driver is designed to produce a nominal 6-volt clock swing, which meets the aforementioned timing criteria, when driving the design load of 70 pf (coupling transistor gates, buses, clamps, and package capacitance). Simulations show that the reset clock driver will operate satisfactorily over a wide variation in amplitude and pulse positioning of ϕ_T and ϕ_T'.

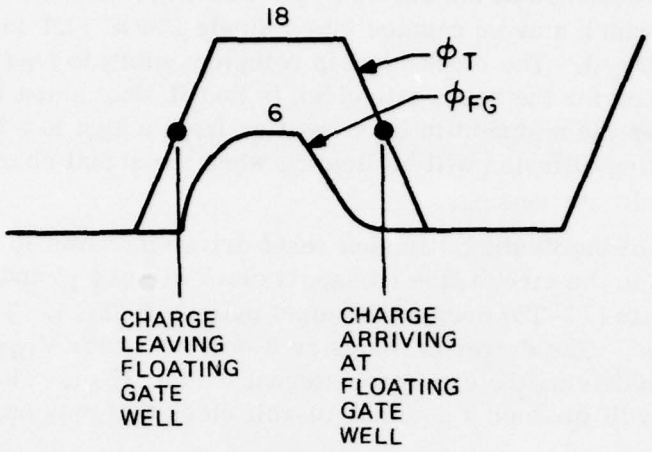


Fig. 3-15. Timing relationship of transfer clock to floating gate reset clock.

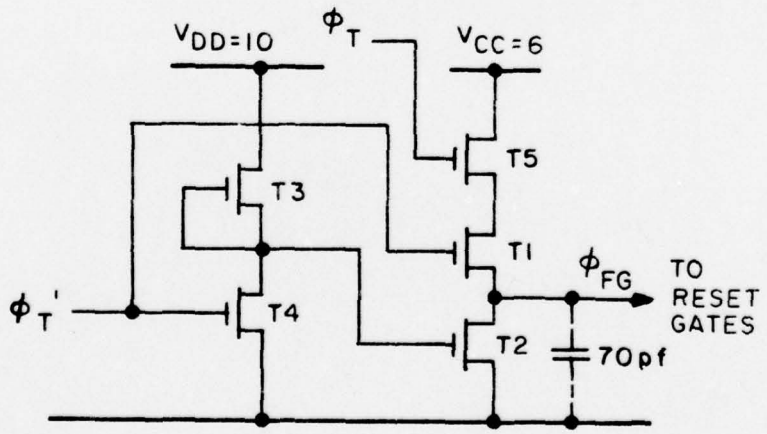


Fig. 3-16. Floating gate reset clock driver circuit.

3.8 FLOATING DIFFUSION RESET CLOCK

The reset gate clock driver produces a clock pulse that may be employed in resetting the floating diffusion at the output of the CCD register. The driver creates a clock pulse ($\phi_{RG'}$) which may be coupled into a single DMOS FET inverter to produce the reset gate clock (ϕ_{RG}). The clock $\phi_{RG'}$ is complementary to ϕ_T (Fig. 3-17). The important criterion for the reset gate clock is that it start going low before the transfer clock reaches the midpoint in its transition from a high to a low level. This assures that the floating diffusion will be floating when the signal charge from the 512th stage is available for sensing.

The schematic of the floating diffusion reset driver is shown in Fig. 3-18. There are two inputs to the circuit: the transport clock signal $\phi_{T'}$ and the buffer output ϕ_T. A NOR gate (T3-T5) drives the output pull-up FET T1. The pull-down FET is enabled by $\phi_{T'}$. The driver develops an 8-volt swing for V_{DD} = 16 volts and V_{CC} = 10 volts, when driving the expected external load of 17 pf. The selected DMOS FET inverter will produce a nominal 10-volt clock that may be biased to an appropriate dc level.

The use of this driver is an alternate method for resetting the floating diffusion. The most straightforward method is to employ the transfer clock (ϕ_T) with an appropriate bias.

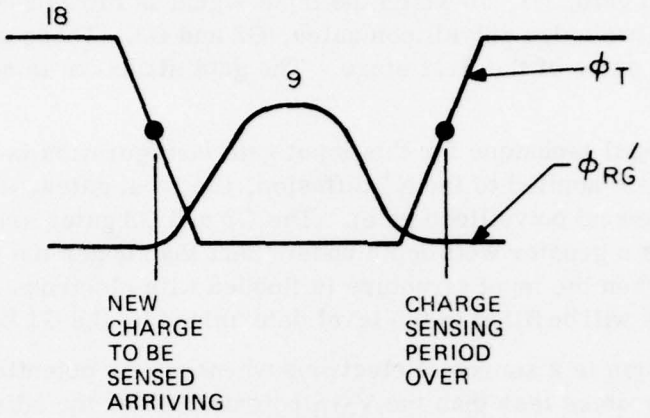


Fig. 3-17. Timing relationship of transfer clock to floating diffusion reset clock.

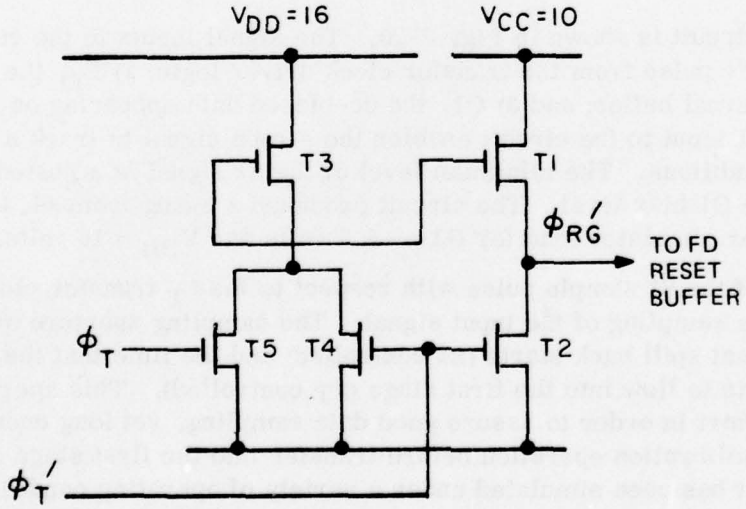


Fig. 3-18. Floating diffusion reset clock driver circuit.

3.9 INPUT SAMPLING (STROBE) CIRCUIT

The input sampling, or strobe, circuit provides an optimum sampling pulse to the input structure of the CCD register. The circuit generates a sampling pulse (S1) designed to accommodate a buried channel input structure, employing the fill and spill input technique.[6,7,8] The S1 pulse is introduced to the input structure on an N^+ diffusion at the beginning of the CCD channel. The N^+ diffusion is followed by the first polysilicon gate, G1, on which the input signal is introduced. The G1 gate is followed by two more polysilicon gates, G2 and G3. These gates, in turn, are followed by the gates of the first stage. The gate structure is shown in Fig. 3-19.

The fill and spill technique for this input gate configuration is controlled by the relative potentials applied to the N^+ diffusion, the input gates, and the first ϕ_T transfer gate (second polysilicon gate). The G2 and G3 gates are dc-biased so that there is always a greater well depth under them than under the signal-modulated gate, G1. Thus, when the input structure is flooded with electrons and then drained, the G2 and G3 wells will be filled to the level determined by the G1 barrier height.

The N^+ diffusion is a source of electrons whenever its potential (with respect to the substrate) becomes less than the V_{MB} potential under the adjacent G1 gate. Conversely, the N^+ diffusion becomes a sink for electrons when its potential is greater than the V_{MB} potential under the G1 gate. The strobe (S1) pulse is designed to reach a minimum potential sufficient to 'flood' the input wells with charge, yet not go so low that charge is spilled down the channel over the barrier of the ϕ_T gate (when ϕ_T is low). Subsequently, the strobe pulse reaches a great enough amplitude to assure that the excess charge will flow back into the diffusion. In this manner, the input structure will 'fill' with carriers and then 'spill' back across the G1 barrier in an equilibration operation that will leave an amount of charge under the G2 and G3 gates proportional to the modulated G1 barrier height.

The strobe circuit is shown in Fig. 3-20. The signal inputs to the circuit are: 1) ϕ_T", a logic pulse from the transfer clock driver logic; 2) ϕ_T, the transfer clock from the external buffer; and 3) G1, the dc-biased data appearing on the G1 input gate. The G1 input to the circuit enables the strobe signal to track a variety of input biasing conditions. The minimum level of the S1 signal is adjusted commensurate with the G1 bias level. The circuit produced a swing from +4.4 volts to +12.8 volts under simulated load for G1 = -3.5 volts and V_{DD} = 16 volts.

The timing of the S1 sample pulse with respect to the ϕ_T transfer clock is critical to accurate sampling of the input signal. The sampling aperture occurs between the time that spill back starts (S1 controlled) and the time that the charge in the G3 well starts to flow into the first stage (ϕ_T controlled). This aperture period should be short in order to assure good data sampling, yet long enough to complete the equilibration operation before transfer into the first stage occurs. The TC1235 circuit has been simulated under a variety of operating conditions, including ϕ_T delay variation. These simulations show that the circuit will accomplish the required timing, and will come close to the 12-nsec aperture period deemed optimum (see Fig. 3-21).

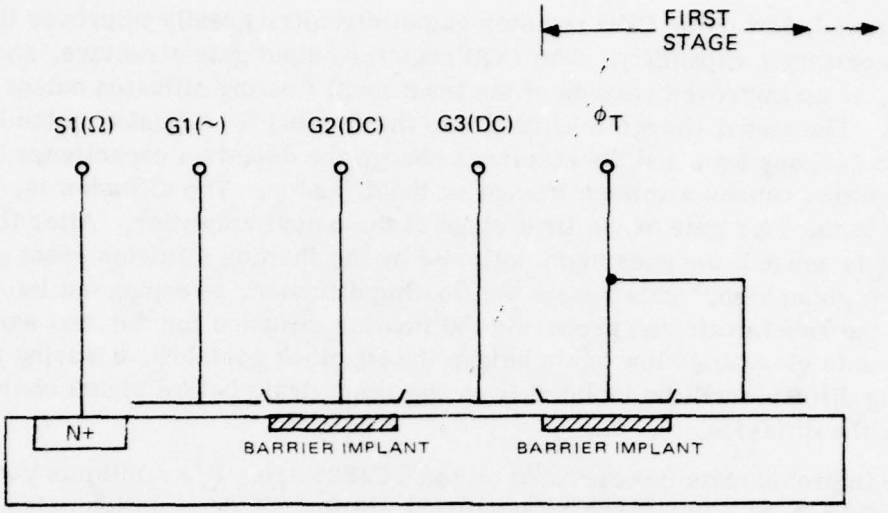


Fig. 3-19. Input sampling gate structure.

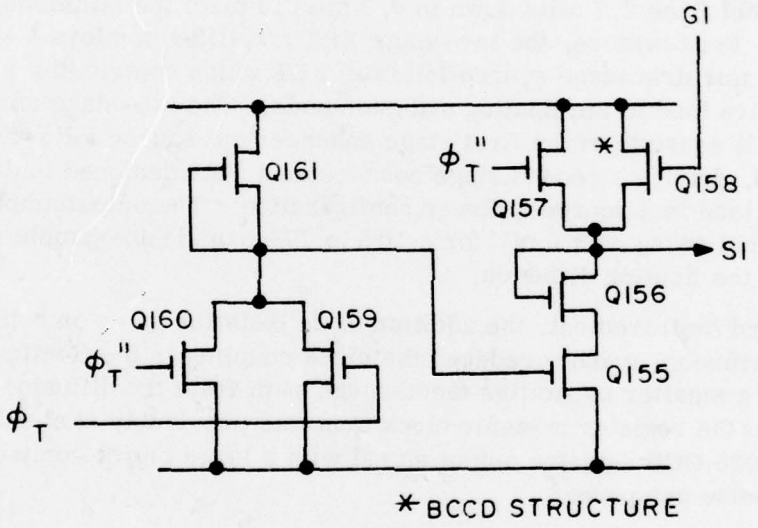


Fig. 3-20. Strobe circuit.

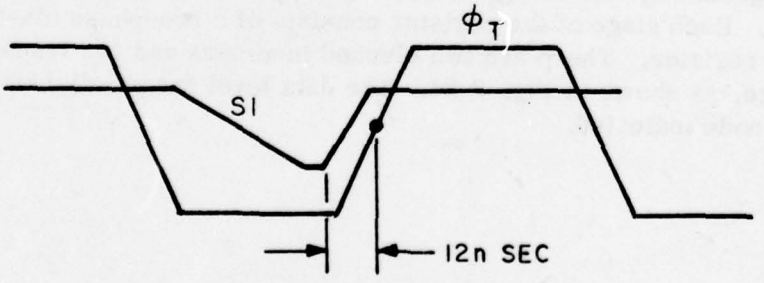


Fig. 3-21. Input sampling pulse.

3.10 CCD REGISTER OUTPUT

Improved, low noise CCD register output circuitry greatly improves the register monitoring capability. The CCD register output gate structure, shown in Fig. 3-22, is an improved version of the traditional floating diffusion output configuration. The signal charge is shifted into the floating N^+ diffusion in the buried layer when ϕ_T goes low, and the electrons charge the depletion capacitance of the diffusion, which causes a voltage change on the diffusion. The diffusion is, in turn, connected to the FET gate of the first stage of the output amplifier. After the signal charge is sensed, ϕ_T goes high, followed by the floating diffusion reset gate clock (ϕ_{RG}) going high. This resets the floating diffusion, sweeping out the signal charge to the reset drain and preparing the floating diffusion for the next sample. The reset gate clock goes low again before the ϕ_T clock goes low, ensuring that the floating diffusion will be isolated from the reset drain before signal charge arrives at the diffusion.

The improvements incorporated on the TC1235 are: 1) a minimum geometry floating diffusion; 2) a two-stage FET output amplifier; 3) dc isolation gates on both sides of the floating diffusion. The floating diffusion node has a total capacitance of only 0.20 pf at 12 volts reverse bias. This was achieved by narrowing the CCD channel from 2.2 mils down to 0.7 mils to meet the minimum geometry N^+ diffusion. Furthermore, the two-stage FET amplifier employs a small 0.4 mil × 0.6 mil first stage source follower FET which contributes a relatively small capacitive load to the floating diffusion node. The two-stage amplifier (see Fig. 3-23) consists of the first stage enhancement source follower with a depletion load, driving a second stage enhancement FET designed to drive a 1K, 6-pf external load in a source follower configuration. The output amplifier will produce a signal swing of 370 mV for a 10% to 70% sample-to-sample charge fluctuation at the floating diffusion.

The third improvement, the addition of dc isolation gates on both sides of the floating diffusion, greatly reduces the clock coupling to the floating diffusion. There is now a smaller capacitive feedthrough path from the diffusion to the reset gate clock and the register transfer clock than was previously attained. The result is a TC1235 CCD register output signal with a large signal component and a small clock noise component.

3.11 PROGRAM REGISTER

The program register design allows high speed serial-to-parallel loading of the latches. Each stage of the register consists of a two-phase six-transistor dynamic shift register. There are two clocked inverters and two transmission gates per stage, as shown in Fig. 3-24. The data level for parallel transfer is sensed at the node indicated.

The 512 stages of the program register are partitioned into a top and a bottom set of 256 stages each. This partitioning allows parallel loading of the two sets. The parallel loading option results in a 50% decrease in the time required to load all the latches, compared with the time required if serial loading were employed.

Each of the 256-stage registers has a TTL-to-MOS translator at the input and a two-stage buffer at the output. The input allows standard TTL logic elements to generate the reference code to be shifted in the registers. The output buffers allow cascading of the program registers (for serial loading) and facilitate monitoring of the program register outputs. The buffers are designed to produce a 7.5-volt swing (one bit to adjacent bit) when driving a 10-pf load (V_{DD} = 10).

The program register is designed to operate at a 5-MHz clock rate, when driven by complementary clocks of 9 volts amplitude at V_{DD} = 10 volts. These operating voltages ensure both valid data transmission down the program register and proper loading of the reference latches.

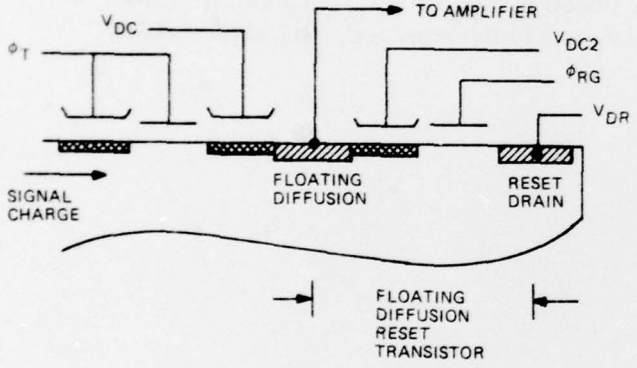


Fig. 3-22. Register output gate structure.

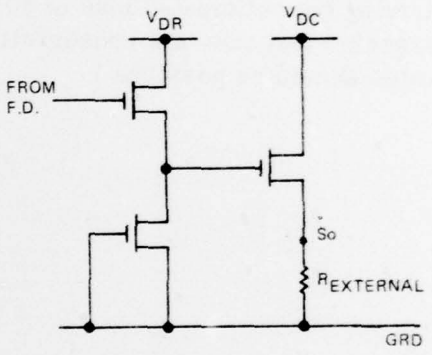


Fig. 3-23. Two-stage output amplifier.

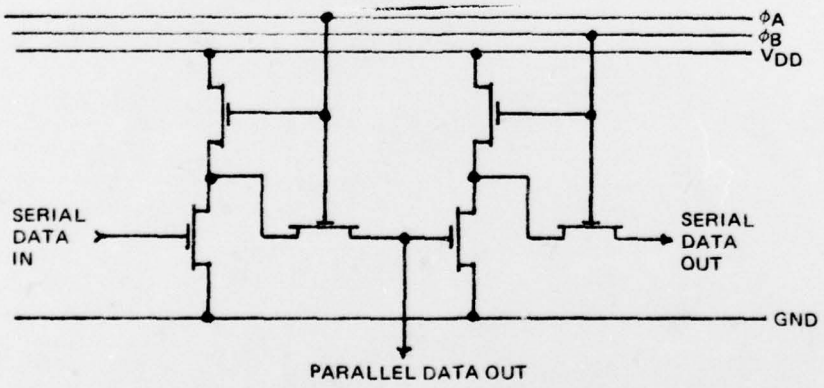


Fig. 3-24. One bit of program register.

3.12 PROGRAM REGISTER DRIVER

The program register driver provides the complementary 5-MHz clocks (ϕ_A and ϕ_B) required for operation of the program register. The driver has a TTL-to-MOS level translator (T43-T48) to accommodate a TTL generated oscillator clock signal (see Fig. 3-25). Thus, a TTL oscillator signal to the program register driver and TTL reference code data inputs to the program registers are the only signals required to shift the reference codes through the program registers.

The driver is configured about two NOR gates (T9-T13 and T31-T35) which ensure that ϕ_A and ϕ_B are complementary and nonoverlapping. The output driver stages for each phase have a V_{CC} supply bus separate from the V_{DD} supply to allow maximum flexibility in operating characteristics. The output stage pull-up transistors are driven by delayed bootstrap circuits (T25-T30 and T3-T8), which develop drive pulses of high amplitude and fast rise and fall times. The other stages of the driver are depletion load or bootstrapped inverters that develop the pulse timing required by the circuitry.

The driver is designed to generate 5-MHz, 9-volt clock waveforms when driving the anticipated load of 80 pf per phase at $V_{DD} = V_{CC} = 10$ volts. (It is expected that this is a conservative estimate of performance, and higher clock rates should be possible.)

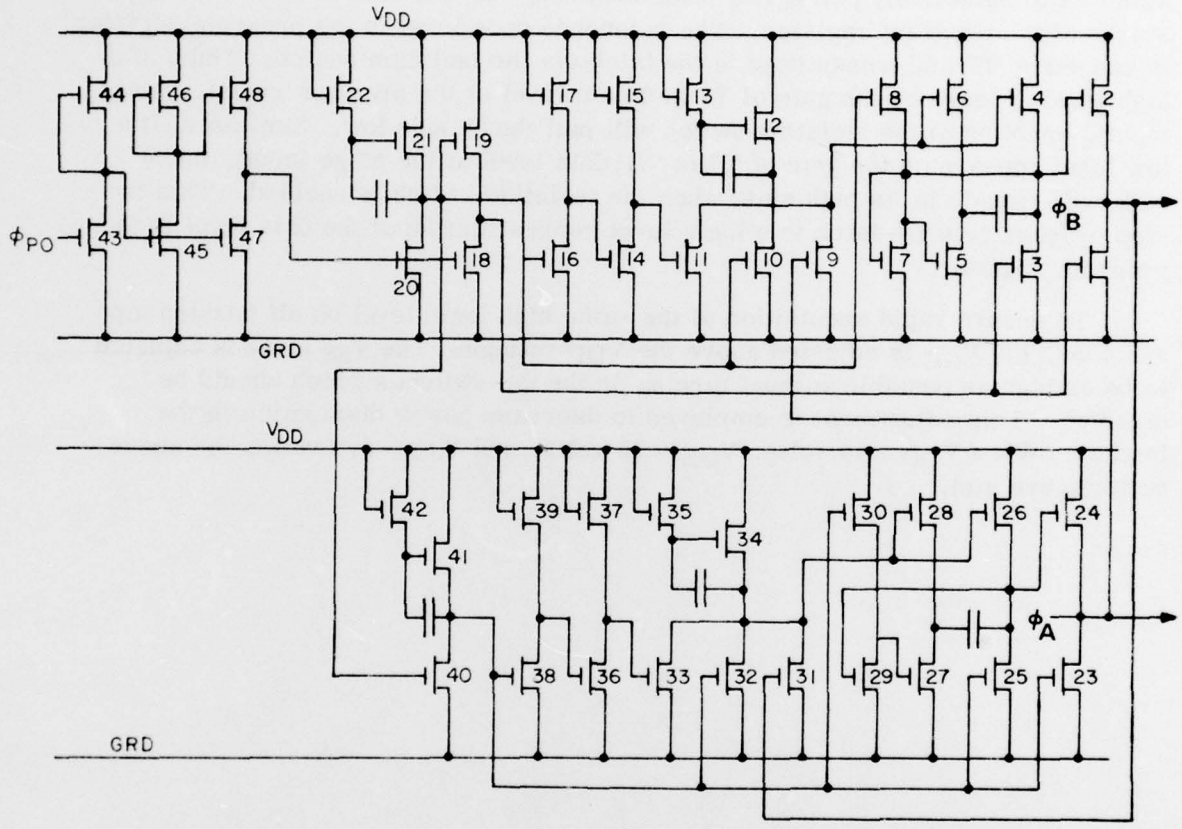


Fig. 3-25. Program register driver circuit.

3.13 BINARY LATCHES

The binary latches provide complementary, stable logic voltage levels to the tap switches. Each latch is composed of a 4-transistor flip-flop with reset and isolation transistors (see Fig. 3-26). The latch is set according to the respective reference code levels present in the program register stages. The actual latch loading sequence requires a combination of a reset action and an isolation switch enabling action.

The load scenario starts with a reset pulse on the gate of the reset transistor (T6). This pulse pulls the $\overline{Q}$ node low, causing the Q node to go high. The next action is to selectively pull Q low commensurate with the data level in the respective stages of the program register. The reference code level in the program register is sensed by T7 and transmitted to the latch via the isolation switch. Thus, if a high level appears on the gate of T7 (a 0 data level at the program register stage input), enabling of the isolation switch will pull the Q node low. Similarly, if a low level appears on the gate of T7 (a "1" data level at the stage input), the Q node will remain in its high state when the isolation switch is enabled. This two-step process sets the latch to a logic level representative of the data level in the program register.

To ensure rapid acquisition of the same high logic level on all enabled tap switches, the V_{GG} is adjusted above the V_{DD} voltage. The V_{SS} level is adjusted to be as high as possible without turning on the tap switches which should be disabled. This adjustment is employed to decrease power dissipation in the latches. When V_{DD} = 10 volts, V_{GG} = 16 volts, and V_{SS} = 3.5 volts, the above criteria are met.

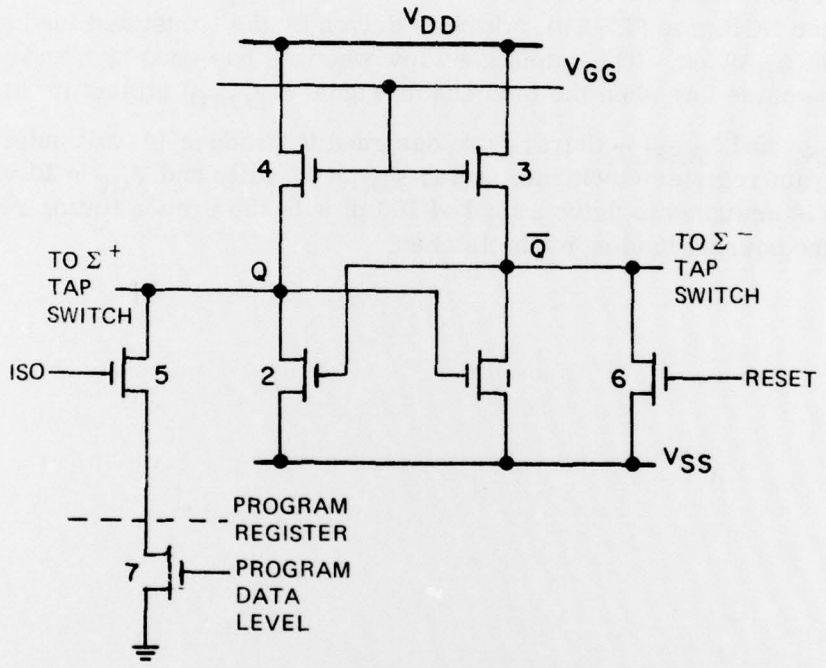


Fig. 3-26. Isolation switch and binary latch circuit.

3.14 LOAD LOGIC

The load logic and drivers greatly reduce the off-chip support circuitry required to load the reference code. The load circuitry accepts a single TTL pulse of duration equal to one bit of data, and generates the required load signals (ϕ_{RESET} and ϕ_{ISO}). The input signal (ϕ_{LOAD}) should occur at a time when the reference code has completely filled the program register. The load enable signal should be a negative going pulse with its leading edge coincident with the ϕ_B falling edge (see Fig. 3-27).

The circuitry used to generate the ϕ_{ISO} pulse is identical to that used to generate the ϕ_{RESET} pulse, with the exception of the input signals. The ϕ_{ISO} pulse enables the isolation switches that act as transmission gates between the program registers and the latches. The ϕ_{RESET} pulse enables the reset transistors on the latches. The circuit for the ϕ_{RESET} pulse is shown in Fig. 3-28. The output is high when the load enable is low and the ϕ_B clock is low. This is ensured by the NOR gate (T7-T9), which is driven by the translated load enable signal and the ϕ_B clock. The output goes low when ϕ_B has gone high and ϕ_A is low. The output remains low when the load enable signal (ϕ_{LOAD}) attains its high level.

The ϕ_{ISO} and ϕ_{RESET} drivers are designed to produce 10-volt pulses at a 5-MHz program register clock rate, when V_{DD} = 16 volts and V_{CC} = 10 volts. Each driver is designed to drive a load of 160 pf with the proper timing relationship to assure correct loading of the latches.

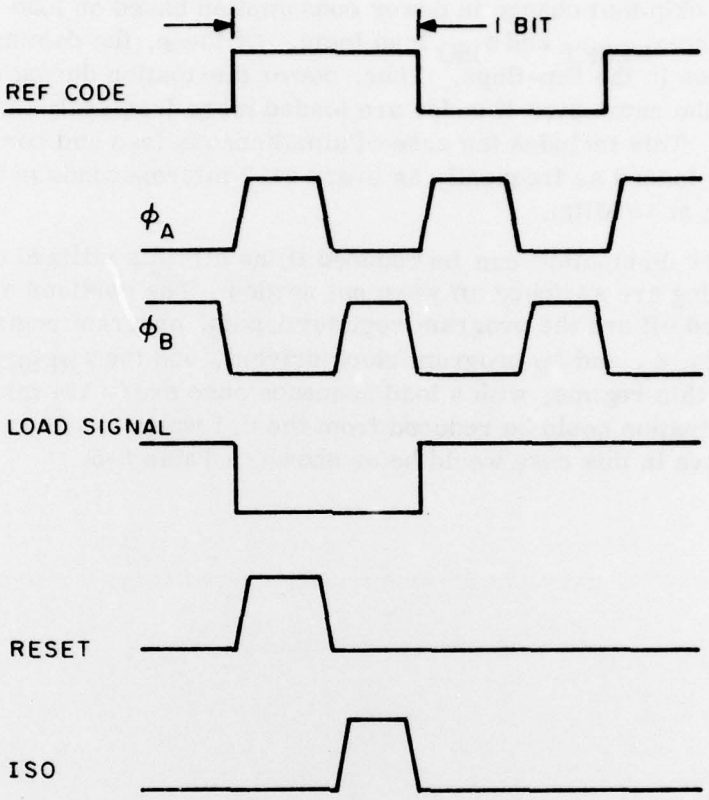


Fig. 3-27. Load sequence signals.

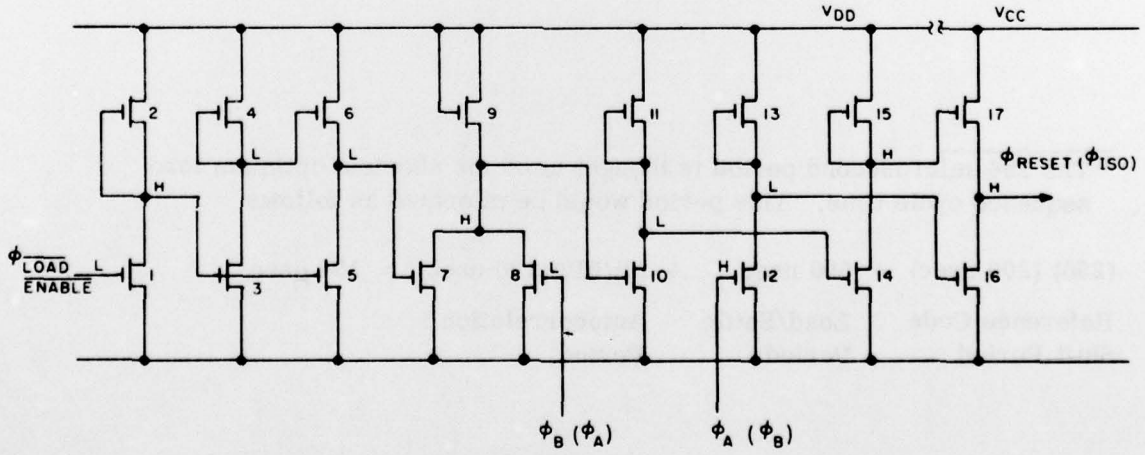


Fig. 3-28. Reset pulse circuit.

3.15 POWER DISSIPATION

The estimated on-chip power dissipation for the TC1235 is detailed in the accompanying tables. Table 3-4 gives the power dissipation for continuous operation of the CCD at 10 MHz with the program register at 5 MHz. This table is based on a reference code load sequence once every 154 microseconds.* The sections of the chip that change in power consumption based on load rate are the flip-flops and the ϕ_{RESET} and ϕ_{ISO} load logic. Of these, the dominant term is static dissipation in the flip-flops. Thus, power dissipation during code load will be essentially the same even if codes are loaded more frequently than every 154 microseconds. This includes the case of simultaneous load and correlate when codes might be loaded as frequently as every 51.2 microseconds (with the CCD register operating at 10 MHz).

The power dissipation can be reduced if the circuits utilized only for reference code loading are switched off when not needed. The portions of the chip that may be switched off are the program register inputs, program registers, program register outputs, ϕ_A and ϕ_B program clock drivers, and the ϕ_{RESET} and ϕ_{ISO} load logic. In this regime, with a load sequence once every 154 microseconds, the power dissipation could be reduced from the 2.1 watts to 1.6 watts. The power breakdown in this case would be as shown in Table 3-5.

---

* The 154-microsecond period is thought to be the shortest optimum load sequence cycle time. This period would be allocated as follows:

(256) (200 nsec)	+ 500 nsec	+ (2)(512)(100 nsec)	= 154 μsec
Reference Code Shift Period	Load/Settle Period	Autocorrelation Period	

TABLE 3-4. TC1235 ON-CHIP POWER DISSIPATION

		P (mW)
Central Array		
CCD Input Structure		0
CCD Register		40
CCD Output Amplifier		13
Tap Structure		502
Flip-Flops*		250
Isolation Switches		0
Program Register Inputs		20
Program Registers		181
Program Register Outputs		18
	Subtotal	1024
Clock Logic and Drivers		
ϕ_T and Strobe (S1)		425
ϕ_{FG} (Floating Gate Reset)		92
ϕ_{RG} (Floating Diffusion Reset)		21
ϕ_A and ϕ_B Program Clocks		190
ϕ_{RESET} and ϕ_{ISO} Load Logic*		362
	Subtotal	1090
	TOTAL	2.114 W

TABLE 3-5. POWER DISSIPATION WITH REFERENCE CODE LOADING CIRCUITS SWITCHED OFF WHEN NOT IN USE

		P (mW)
Central Array		
CCD Input Structure		0
CCD Register		40
CCD Output Amplifier		13
Tap Structure		502
Flip-Flops*		250
Isolation Switches		0
Program Register Inputs		6.7
Program Registers		60.6
Program Register Outputs		6.0
	Subtotal	878.3
Clock Logic and Drivers		
ϕ_T and Strobe (S1)		425
ϕ_{FG} (Floating Gate Reset)		92
ϕ_{RG} (Floating Diffusion Reset)		21
ϕ_A and ϕ_B Program Clocks		63.7
ϕ_{RESET} and ϕ_{ISO} Load Logic*		121.3
	Subtotal	723.0
	TOTAL	1.601 W

*If a reference code load sequence occurs every 154 μsec.

The TC1235 was designed to minimize not only the number of signals required for operation, but also the number of power supply voltages. There are 61 I/O pads on the chip. They are listed in Table 3-6 in the order in which they are to be bonded out to the Kyocera package. A diagram of the pad locations, showing the metal pattern, is given in Fig. 3-29.

The asterisks in the table indicate pads requiring signal inputs from the external system. The required system input signals are:

(12) Program Register Input #2

(32) G2 (Variable dc Input Gate)

(33) G3 (Variable dc Input Gate)

(38) Program Register Input #1

(40) G1 (CCD Signal Input)

(41) ϕ_{MO} (CCD Master Oscillator)

(50) ϕ_{LOAD} (Program Load Enable)

(55) ϕ_{PO} (Program Master Oscillator)

The other signals in the table are generated on-chip, to be fed back to the chip in response to the eight input signals.

The required power supply voltages are:

Pin Nos.	V_{DC}
20	28 volts
19, 42, 52, 61	16 volts
8, 9, 15, 24, 36, 37, 43, 46, 54, 57	10 volts
2, 3, 4	6 volts
18	-2 volts

TABLE 3-6. TC1235 I/O PADS

Pad Designation	Voltage
1. ΣV_{SS}	GRD
2. ϕ_{DC} (CCD Register)	+6
3. V_{BIAS}	+6
4. ΣV_{DD}	+6
5. Σ^-	
6. Σ^+	
7. V_{SSFF}	GRD
8. V_{DDFF3}	+10
9. V_{DDFF4}	+10
10. N/C	
11. ϕ_{RESET} (In)	0 to +9
12. PR_{IN2}*	0 to +4
13. ϕ_B (In)	0 to +9
14. ϕ_A (In)	0 to +9
15. V_{DD} (Prog. Reg.)	+10
16. N/C	
17. GRD	GRD
18. SUB	-2
19. ϕ_{DC} (Output Amp.)	+16
20. V_{DD} (Output Amp., Output Drain)	+28
21. PR_{OUT2}	
22. ϕ_{ISO} (In)	0 to +9
23. N/C	
24. V_{DDFF5}	+10
25. Σ^+	
26. Σ^-	
27. ΣV_{SS}	GRD
28. ϕ_{RG} (In)	-6 to +12
29. S_o	[910 Ω]
30. ϕ_T (In)	-3 to +15
31. ϕ_{FGR} (In)	6 to 12
32. G2*	+6

Pad Designation	Voltage
33. G3*	+3.1
34. Σ^-	
35. Σ^+	
36. V_{DDFF2}	+10
37. V_{DDFF1}	+10
38. PR_{IN1}*	0 to +4
39. S1	
40. G1*	-3 to -0.5
41. ϕ_{MO} (CCD)	0 to +4
42. V_{DD} (ϕ_T, S1)	+16
43. V_{CC} (ϕ_T)	+10
44. ϕ_T' (Out)	
45. ϕ_{RG}' (Out)	
46. V_{DD} (ϕ_{FGR})	+10
47. ϕ_T (In)	-3 to +15
48. ϕ_{FGR} (Out)	
49. ϕ_{ISO} (Out)	
50. $\phi_{\overline{LOAD}}$ (In)*	+4 to 0
51. ϕ_{RESET} (Out)	
52. V_{DD} (Logic)	+16
53. ϕ_B (Out) (In)	0 to +9
54. V_{CC} (Prog. Dr./Load)	+10
55. ϕ_{PO} (Program)*	0 to +4
56. ϕ_A (Out) (In)	0 to +9
57. V_{DD} (Prog. Reg./Dr.)	+10
58. PR_{OUT1}	
59. ϕ_{ISO} (In)	0 to +9
60. ϕ_{RESET} (In)	0 to +9
61. V_{GGFF}	+16
62. Σ^+	
63. Σ^-	
64. ΣV_{GG}	+2.4

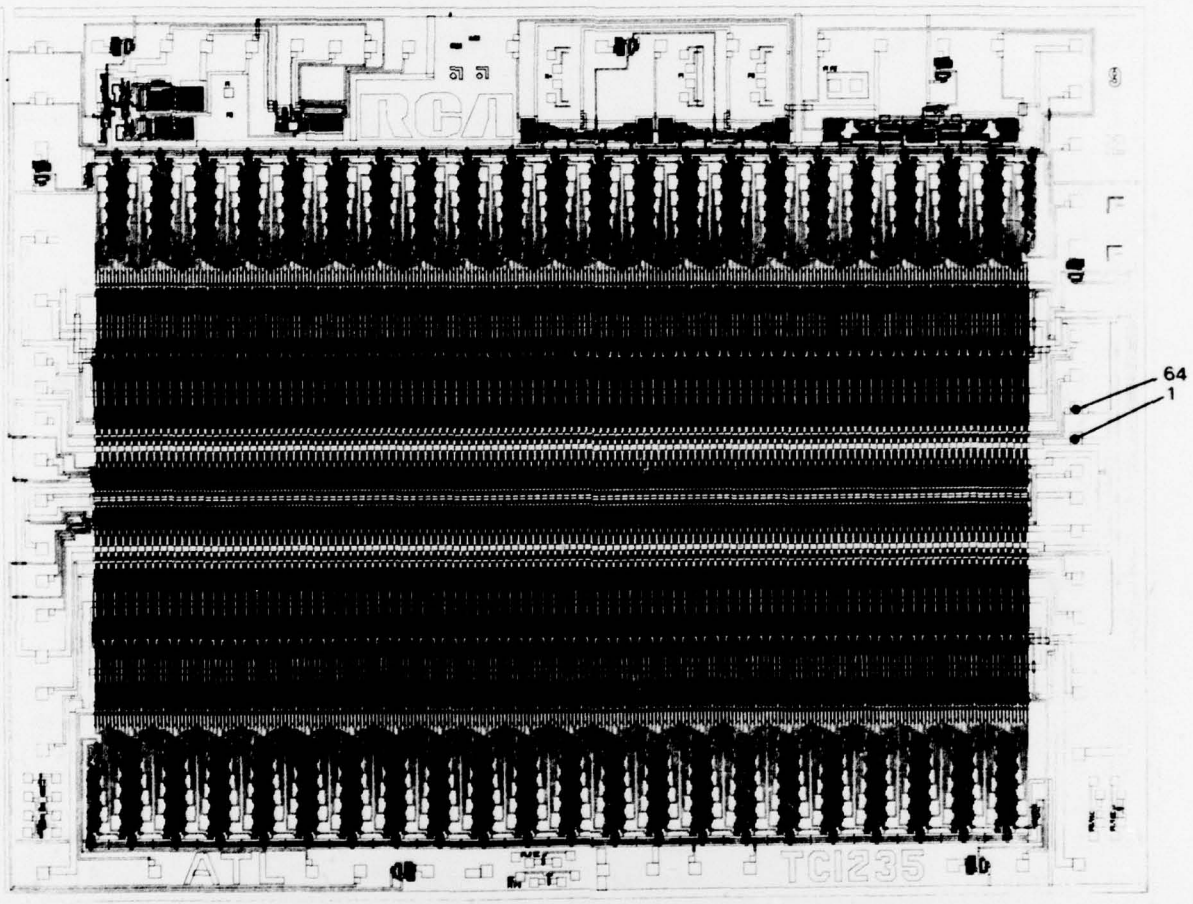


Fig. 3-29. Metal and poly-Si levels of TC1235 correlator chip.

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